PC Engines

ALIX.3c3 / alix.3d3 system boards

PC Engines GmbH
www.pcengines.ch

Table of contents

Federal Communications Commission Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio energy. If this equipment is not installed and used in accordance with the manufacturer's instructions, it may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.

- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

This board is designed for installation in a shielded enclosure (metal or plastic with conductive coating). Shielded cables are required on LAN and serial ports to assure compliance with FCC regulations.

A copy of the test report will be provided on request.

CE Declaration of Conformity

We, PC Engines GmbH, declare that ALIX.3 series boards, when installed in PC Engines metal enclosures (box2c), are in conformance with:

- EN 61000-6-3 (2005)   (emissions, residential and industrial)

- EN 61000-6-2   (ESD, susceptibility, residential and industrial)

The unit under test is in conformity with the standards mentioned above. A copy of the test report will be provided on request.

Compliance information

For FCC, ALIX has been tested as a CPU board, installed in an enclosure, with the top cover removed. No further testing should be required if the board is used with other FCC tested modular components. Please see http://www.fcc.gov/oet/ for more details. The responsible party for FCC is the importer.

Testing for CE mark must be done at the level of the complete product, possibly including the wireless cards. Please contact PC Engines for assistance and documentation.

For satisfactory resistance to electrostatic discharge events (ESD), the ALIX board should be grounded (e.g. through the mounting holes, or the serial port connector).

Recycling / disposal
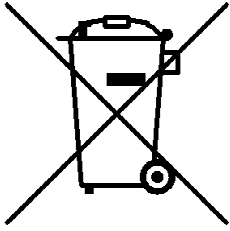
Do not discard electronic products in household trash!

All waste electronics equipment should be recycled according to local regulations.

Information for the recycler:

Please cut off Lithium battery, if present, for separate recycling.

PC Engines enclosures are made of aluminium.

ALIX.3d3 features

PC Engines ALIX boards are small form factor system boards optimized for wireless routing and network security applications.

- AMD Geode LX CPU, 500 MHz (LX800) 5x86 CPU
- 256 KB cache (64K data + 64K instruction + 128K L2)
- 1 Ethernet channel (Via VT6105M, 10 / 100 Mbit/s)
- 2 miniPCI sockets for 802.11 wireless cards and other expansion
- 256 MB DDR SDRAM, 64 bit wide for high memory bandwidth
- 512 KB flash with Award BIOS
- CompactFlash socket for user's operating system and application
- 7 to 20V (absolute maximum, recommend 18V) DC supply through DC jack or passive power over Ethernet. Suggest a 18V / 15W supply. Center pin = positive, sleeve = ground, 2.1 mm diameter.
- 1 serial port (DB9 male)
- 2 USB 2.0 ports
- Header for LPC bus (use for flash recovery or I/O expansion)
- Temperature range 0 to 50°C
- Dimensions 100 x 160 mm
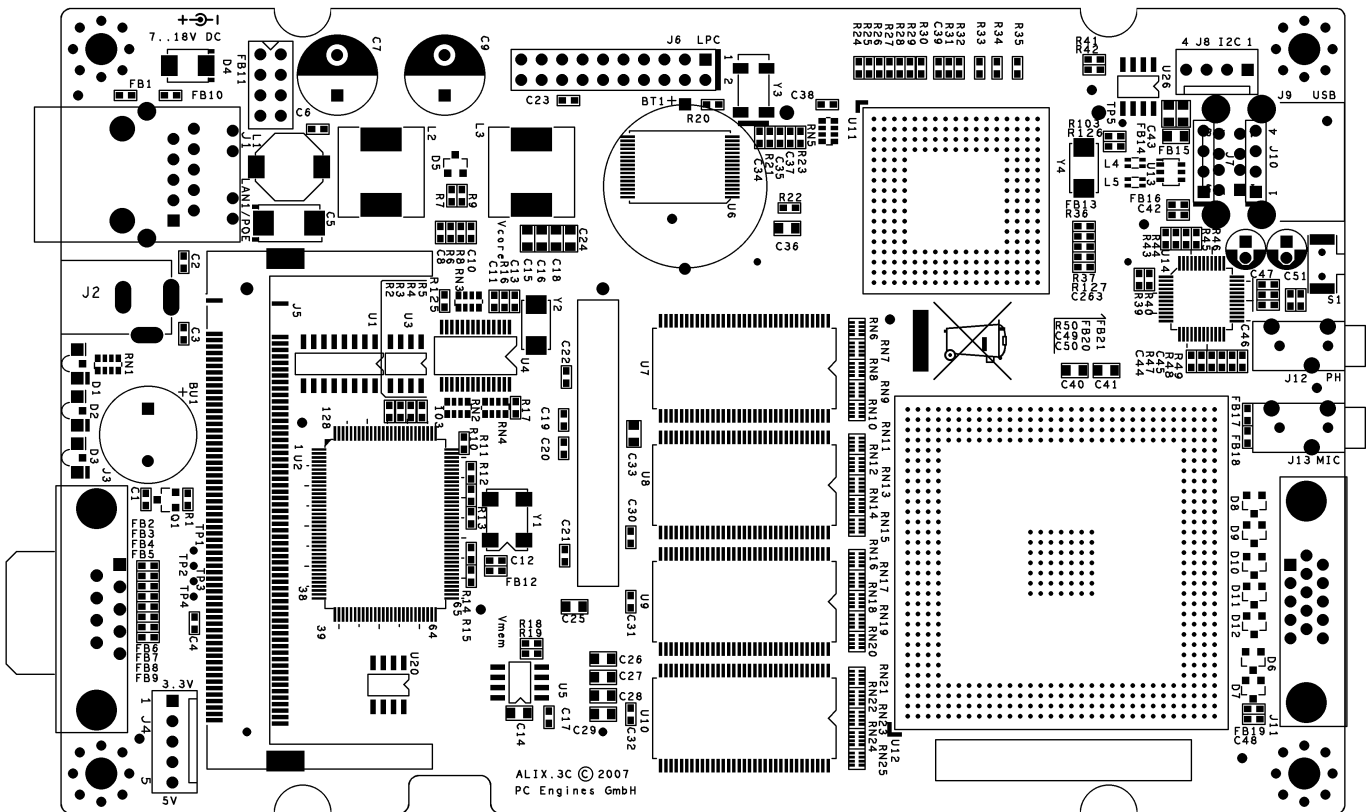
OEM options

The following options can be configured for larger orders:

- CMOS level serial port (RXD / TXD only)
- Optional header for I2C bus
- Optional buzzer for "beeps"
- Optional pushbutton switch

Getting started…

- Connect VGA, keyboard and mouse as needed. If using a USB hub, the keyboard should be connected to the first port (BIOS issue).

- Insert a bootable CF card. Hot swap of CF cards is not supported !

- Connect a DC power supply to the DC jack J2. 2.1 mm center pin = positive, sleeve = ground. Power supply should be able to supply at least 10W power output. To avoid arcing, please plug in the DC jack first, then plug the adapter into mains.

There is no power switch, the system will start as soon as power is connected. You should now see BIOS startup messages.

Setup options

ALIX.3d3 uses Award BIOS for more features and operating system compatibility. Press **Delete** during startup to enter setup.

Press **Escape** to get a boot menu.

Please do not enable the second COM port – this will interfere with the VGA monitor ID functions.

USD CD-ROM or DVD

Award BIOS can boot from USB devices. BIOS time-outs are a bit short – if this happens please press Pause during startup, then Escape to enter the boot menu.

BIOS upgrade

The current BIOS can always be found at www.pcengines.ch/alix3d3.htm . To upgrade, boot from a CF card to FreeDOS (see www.pcengines.ch/freedos.htm) , then execute the flash upgrader (sb.com).

Do not turn off power while the flash upgrade is running, otherwise the flash BIOS may be corrupted. If this happens, the board can be revived using an LPC adapter available from PC Engines.

Hardware compatibility

Commell MP-541D miniPCI dual Ethernet card will not work. This card uses another ID select line for the second Ethernet channel, which the BIOS does not know about, and violates the PCI specification.

Cologne HFC-S ISDN does not work on Geode LX.

To reduce standby power draw, Ethernet Wake on LAN is not supported.

Due to limitations in the AMD CS5536 companion chip, the serial port only supports RXD / TXD, not the handshake signals.

Power over Ethernet

ALIX implements a passive power over Ethernet scheme, using the unused pairs of LAN1 for power. Power can be injected using a passive POE splitter such as PC Engines POE.1A. .

ALIX is NOT compatible with 48V / IEEE 802.3af POE. Please use an external splitter if required.

When power is fed in through POE, it is possible to "steal" unregulated power through the DC jack. Please note that this port is not fused. The POE input diode is rated for a current of 2A.

Software issues

With older BIOS versions, Linux boot may hang for ~ 30 minutes if no monitor is attached. This problem is caused by the VESA DDC (monitor ID) code in the BIOS. Please update to the current BIOS version if you encounter this issue.

Please note that this board is "legacy free", and does not include a keyboard controller. Some boot loaders will hang, waiting for the keyboard controller to be ready.

MFGPT high resolution timer

Incorrect use of the CS5536 MFGPT (multi function timer) can hang the board. If in doubt, please disable this option in your kernel.

Common drivers for the MFGPT use the timer with the 32768 Hz time base, resulting in a 1024 Hz tick rate. This will result in time drift when HZ = 1000. Please fix this, or install adj-timex.

BIOS POST codes

The system BIOS writes POST / diagnostic codes to port 80h. To make these codes visible, use a miniPCI POST card such as PC Engines POST.5A. A POST code table can be found at:

      http://www.bioscentral.com/postcodes/awardbios.htm -> look for version 4.51PG

Support

Please email support@pcengines.ch.

ALIX block diagram

Full board schematics are available online !
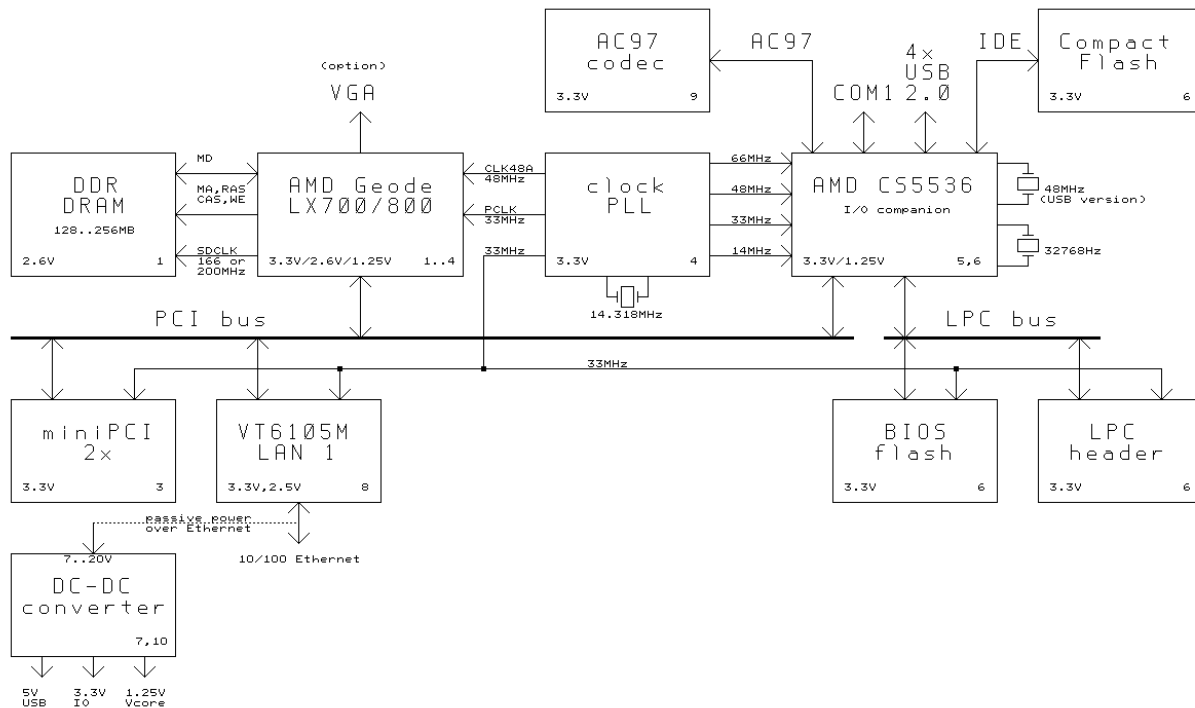
ALIX connector pinouts

J3   COM1 serial port

The standard PC pinout is used. To connect to a PC, use a null modem or "Laplink" cable. Due to limitations of the AMD CS5536 companion chip, handshake signals are not connected.

1	DCD	data carrier detect (input)	- not available on CS5536
2	RXD#	receive data (input)	
3	TXD#	transmit data (output)	
4	DTR	data terminal ready (output)	- driven active
5	GND	ground	
6	DSR	data set ready (input)	- not available on CS5536
7	RTS	ready to send (output)	- driven active
8	CTS	clear to send (input)	- not available on CS5536
9	RI	ring indicator (input)	- not available on CS5536

J17   COM1 serial port (3.3V levels, build option)

This header is available on alix.3d and later. This port is connected in parallel with the MAX3243 RS-232 driver, remove this part if CMOS level serial port is desired as an alternative.

1	V3	3.3V supply
2	TXD	transmit data (output)
3	RXD	receive data (input)
4	GND	ground

J4   COM2 serial port (build option)

This option will interfere with VGA DDC (monitor ID) functions, and must be enabled explicitly in BIOS setup. Signal levels are 3.3V, not RS-232.

1	V3	3.3V supply
2	TXD	transmit data (output)
3	RXD	receive data (input)
4	GND	ground
5	VCC	5V supply

J1   Ethernet port 1

An RJ45 connector with integrated magnetics is used. This port implements a passive power over Ethernet scheme over the two unused pairs. Do not exceed 20V as the TVS protection diode may start clamping above this voltage.

1	TX+	transmit positive
2	TX-	transmit negative
3	RX+	receive positive
4	VIN	power supply (nominal 7 to 20V)
5	VIN	"
6	RX-	receive negative
7	GND	power return
8	GND	"

J9   USB jack

Dual USB 2.0 connections. As a build option, 4 pin headers can be installed instead of the USB connector. The current limit is rather sensitive, consider a self-powered hub when attaching high power devices.

1	VCC	switched +5V supply
2	DATA2-	negative data
3	DATA2+	positive data
4	GND	ground
5	VCC	switched +5V supply
6	DATA1-	negative data
7	DATA1+	positive data
8	GND	ground

J4/J2 / J2   DC power jack

This is a generic DC jack connector with a 2.1mm center pin. Recommended input voltage is +18V.

center	VIN	Positive input voltage
sleeve	GND	Ground

J5, J14 miniPCI socket

These sockets implement the miniPCI interface. Please see schematic for pinout.

J15   CompactFlash

The CompactFlash card is used in True IDE mode. Hot insertion is not supported – please power off the unit before inserting a CF card.

1	GND	ground
2	D3	IDE data
3	D4	IDE data
4	D5	IDE data
5	D6	IDE data
6	D7	IDE data
7	CS0#	IDE decode (1F0..1F7)
8	A10	ground
9	ATASEL#	ground to select true IDE mode
10	A9	ground
11	A8	ground
12	A7	ground
13	VCC	+3.3V power supply
14	A6	ground
15	A5	ground
16	A4	ground
17	A3	ground
18	A2	IDE address
19	A1	IDE address
20	A0	IDE address
21	D0	IDE data
22	D1	IDE data
23	D2	IDE data
24	IO16#	16 bit decode, not connected
25	CD2#	card detect, not connected
26	CD1#	card detect. not connected
27	D11	IDE data
28	D12	IDE data
29	D13	IDE data
30	D14	IDE data
31	D15	IDE data
32	CS1#	IDE decode (3F6..3F7)
33	VS1#	not connected
34	IOR#	IDE read strobe
35	IOW#	IDE write strobe
36	WE#	connected to +3.3V
37	IRQ	IDE interrupt
38	VCC	+3.3V power supply
39	CSEL#	cable select, ground = master
40	VS2#	not connected
41	RESET#	IDE reset, active low
42	IORDY	IDE ready
43	INPACK#	IDE DMA request

44	REG#	IDE DMA acknowledge
45	DASP#	pulled up
46	PDIAG#	pulled up
47	D8	IDE data
48	D9	IDE data
49	D10	IDE data
50	GND	ground

The CompactFlash specification can be found at www.compactflash.org.

J6   LPC expansion

The LPC port is used in the factory to connect an alternate flash BIOS to start the board when the on-board flash is corrupted or blank. Use PC Engines adapter LPC.1A for this purpose if needed.

The LCP port can also be used to connect a super I/O device. Unlike SC1100 based WRAP boards, this port cannot be reprogrammed as GPIO pins. Contact PC Engines for sample schematics if required.

1	LCLK0	LPC clock (33 MHz)
2	GND	ground
3	LAD0	LPC data 0
4	GND	ground
5	LAD1	LPC data 1
6	GND	ground
7	LAD2	LPC data 2
8	GND	ground
9	LAD3	LPC data 3
10	GND	ground
11	LFRAME#	LPC frame
12	GND	ground
13	PCIRST#	reset (active low)
14	CLK48	super I/O clock (48 MHz)
15	ISP	high to use LPC flash, low to use on-board flash, pulled low by resistor
16	VCC	+5V supply
17	GND	ground
18	V3	+3.3V supply
19	SERIRQ	serial interrupt
20	LDRQ#	LPC DMA request

J8   I2C bus (build option)

This optional header can be used to connect user specific hardware, e.g. a front panel microcontroller, or for a licensing dongle. See AMD CS5536 data sheet for programming details.

1	+3.3V	power supply
2	SMB_SCL	I2C clock
3	SMB_SDA	I2C data
4	GND	ground

J12   Headphone out

J13   Microphone in

Starting with alix.3d3, this connector can also be configured to connect to line in. Please see schematics for details, parts marked with – are not populated.

J11   VGA

1	VGAR	VGA red
2	VGAG	VGA green
3	VGAB	VGA blue
4	nc	no connect
5	GND	ground
6	GND	ground
7	GND	ground
8	GND	ground
9	USBVCC	+5V supply (fused)
10	GND	ground
11	nc	no connect
12	DDCDAT	DDC data
13	HS	horizontal sync
14	VS	vertical sync
15	DDCCLK	DDC clock

BT1   RTC battery

CR2032 Lithium battery is soldered in. Please observe correct polarity, top side of the battery is + positive terminal.

For alix.3d and later, also add a jumper on J16 pins 1 to 2. This is the CMOS reset jumper for alix.3d3.

Specification: CR2032, horizontal mount, 20.4 mm lead spacing, for example Renata CR2032FH1 or Panasonic   BR2032-1HE.

J16   CMOS reset jumper

Position 1 – 2 = normal operation.
Position 2 – 3 = CMOS reset.

On alix.3c3, more drastic measures are required to reset CMOS…

BU1   Buzzer (build option)

Optional audio transducer. The footprint fits a Hycom HY-05 or equivalent.

Status LEDs

Status LEDs are all turned on by the BIOS on power up. The BIOS will turn off LEDs 2 and 3 before booting the operating system.

Location	GPIO	read port	write port
LED1 (left)	G6	port 06100h bit 6	port 06100h bit 6 / 22
LED2 (middle)	G25	port 06180h bit 9	port 06180h bit 9 / 25
LED3 (right)	G27	port 06180h bit 11	port 06180h bit 11 / 27

The CS5536 GPIO ports are programmed by 32 bit atomic writes. This avoids the need for read / modify / write operations and the locking issues they entail. For example, to turn off LED1 (high), write 0000'0040h to port 06100h. To turn on LED1 (low), write 0040'0000h. Multiple port bits can be changed at the same time. Again, your code must use 32 bit I/O access ! With the current Award BIOS, additional port initialisation will be required.

Pushbutton switch

The optional mode switch can be accessed by software as follows:

Location	GPIO	read port	
MODESW#	G24	port 061b0h bit 8	(active low, 0 = switch pressed)

With the current Award BIOS, additional port initialisation is required…

Low level programming

Please see www.pcengines.ch/file/alixllc.zip for sample code.