PC Engines Apu3 series system board

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CE declaration of conformity

Supplier's Name:PC Engines GmbHSupplier's Address:Flughofstrasse 58, 8152 Glattbrugg, Switzerlanddeclares, that the productProduct name and model:apu3a2, apu3a4Conforms to the following Product Specifications and Regulations:EMC (EN 301 489-1 V1.9.2 2011-09):EN 55022:2010/AC:2011 Class B (emissions)EN 61000-4-2:2009 (ESD)EN 61000-4-2:2009 (ESD)EN 61000-4-3:2006/A1:2008/A2:2010 (radiated immunity)EN 61000-4-5:2014 (surge immunity)EN 61000-4-5:2014 (surge immunity)EN 61000-4-6:2014 (conducted immunity)

RoHS:

EN 50581:2012

The product herewith complies with the requirements of the EMC directive 2004/108/EC, the RoHS directive 2011/65/EU and carries the CE marking accordingly.

P. Dornier

Pascal Dornier President Glattbrugg, November 16, 2016

Test reports available on request. Please note that further compliance testing at the system level may be required for CE mark when other modules such as wireless cards are added.

Recycling / disposal



Do not discard electronic products in household trash! All waste electronics equipment should be recycled according to local regulations.

Information for the recycler:

Remove the LR44 alkaline battery for separate recycling. Our enclosures are made of aluminium.

Federal Communications Commission Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio energy. If this equipment is not installed and used in accordance with the manufacturer's instructions, it may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This board is designed for installation in a shielded enclosure (metal or plastic with conductive coating). Shielded cables may be required on LAN and serial ports to assure compliance with FCC regulations.

A copy of the test report will be provided on request.

Note: apu has been tested as a CPU board, installed in an enclosure, with the top cover removed. No further testing should be required if the board is used with other FCC tested modular components. Please see http://www.fcc.gov/oet/ for more details. The responsible party for FCC is the importer.

Introduction / Features

PC Engines apu boards are small form factor system boards optimized for wireless routing and network security applications.

СРИ	AMD G series GX-412TC, 1 GHz quad core (Jaguar core) with 64 bit support, AES-NI, 32K data + 32K instruction cache per core, 2MB shared L2 cache
DRAM	2 or 4 GB DDR3-1333 DRAM
Storage	Boot from SD card (built-in adapter, connected through USB), USB or m-SATA SSD. 1 SATA data + power connector.
Power	12V DC, 2.5 mm center pin, center positive. About 6 to 10W depending on CPU load. Recommend 12V adapter rated for at least 1.5A to provide margin for peripherals.
Expansion	3 miniPCI express (two with SIM socket for 3G modem), LPC bus, GPIO header, optional I2C bus, COM2 (3.3V RXD/TXD).
Connectivity	3 Gigabit Ethernet (Intel i210AT / i211AT), 1 DB9 serial port (console).
Firmware	CoreBoot open source system BIOS with support for iPXE and USB boot.
Form factor	6"x6" (152.4 x 152.4 mm), fits in our case1d2*u enclosures.
Cooling	Conductive cooling from the CPU to the enclosure.

Heat spreader assembly

The apu CPU is passively cooled by heat conduction to the enclosure. This requires correct installation of a heat spreader.

The board should not be operated without CPU cooling except for brief bench tests.

The included heat spreaders are designed for our enclosures. Third party enclosures should work if they are made from aluminium, and have a board standoff height of 5 mm. If in doubt, please contact us. Based on our measurements, at full load the CPU runs a few degrees cooler in the black (case1d2blku) or red (case1d2redu) enclosures, compared to the plain anodized enclosure (case1d2u).

Photos for this assembly procedure can be found at <u>www.pcengines.ch/apucool.htm</u>.

- Remove DB9 hex nuts using a suitable tool (such as our hexbit tool, or a simple plier).
- Using a small x-acto knife or similar, peel transparent backing foil from the small blue heat conductive pad. Apply to the CPU. Then peel the blue cover foil from the heat conductive pad.
- Place the alu heat spreader (blank side down) over the CPU. Make sure to avoid conflict with nearby through hole components. Peel the cover foil.
- "Bottoms up" hold the enclosure base upside down, feed the board DB9 and LAN connectors through the openings. Lightly press board and enclosure base together to stick the heat spreader in place.
- Turn around and carefully press down around CPU and heat sink to get good contact between enclosure and heat spreader. Then insert screws and hex nuts.

Please do not disassemble the unit needlessly, the thermal conductive pads are easily damaged. Replacement blue pads (free) or complete heat spreader kits (nominal charge + shipping cost) are available from us on request.

Getting started...

- Please install heat spreader as described in the prior section.
- Insert a boot device (SD card, mSATA SSD, USB stick, or PXE through LAN).
- Connect serial port to a PC through null modem cable (RXD / TXD crossed over). Set terminal emulator to 115200 8N1.
- Connect Ethernet as needed.
- Connect a 12V DC power supply to the DC jack. Power supply should be able to supply at least 18W for some margin. To avoid arcing, please plug in the DC jack first, then plug the adapter into mains.

The board should now power on. All three LEDs will light during BIOS POST, then the system will try to boot. You should see BIOS messages on the serial console. Press F10 for boot device selection. For example:

```
PCengines Press F10 key now for boot menu:
Select boot device:
1. SD card SD04G 3796MiB
2. Payload [memtest]
3. Payload [setup]
```

3/3/2017

Setup options

To set up the boot sequence and other options, press F10 for boot device selection, then select Payload [setup].

```
_____
Type lower case letter to move device to top
_____
boot devices
 a SD Card
 b USB 1
 c USB 2
 d mSATA
 e SATA 2
 f SATA 3
 g NETWORK / PXE
______
Type upper case letter to invoke action
_____
 R Restore boot order defaults
 N Network/PXE boot - Currently Enabled
 S Serial console - Currently Enabled
 E Exit setup with save
 X Exit setup without save
```

The lower case letters will change the boot sequence, pull the selected device to the top of the list.

R toggles serial console enable. Push the switch S1 during startup to get into setup when the serial console is disabled.

Memtest

To start, press F10 for boot device selection, then select Payload [memtest].

(current builds do not react to console inputs)

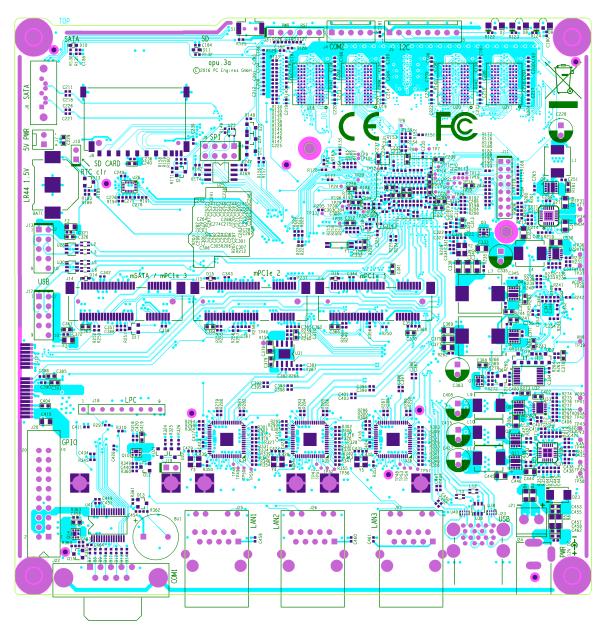
BIOS update

Please see www.pcengines.ch/howto.php.

CoreBoot source code

The CoreBoot firmware is licensed under the GPL. To obtain the source code and a Voyage Linux image with the tool chain needed to compile it, please contact <u>support@pcengines.ch</u>.

Connectors



BAT1 battery	LR44 1.5V alkaline battery for RTC / CMOS
J1 SIM	(bottom side) – SIM socket for 3G modem installed in miniPCIe J15. Can be swapped with J2 SIM under software control.
J2 SIM	(bottom side) – SIM socket for 3G modem installed in miniPCIe J14. Can be swapped with J1 SIM under software control.
J3 power / reset	Pins 1-2 = SPI write protect (requires additional software support to configure SPI flash) Pins 2-3 = power button Pins 4-5 = reset button Pins 5-6 = enable NCT5104D watchdog reset (requires additional software

	support)
J4 COM2	3.3V serial port (RXD / TXD only).
(J5 I2C / LED)	(optional expansion, see schematic for pinout)
J6 SATA	For SATA devices.
J7 SATA power	5V power for SATA devices.
J8 SD card	SD card interface, driven by AMD SOC, use sdhci driver.
J9 SPI	SPI header for debricking. Do not connect pins 7 / 8 for Dediprog use.
J10 CMOS reset	Short these pins while power is off to clear RTC / CMOS RAM. Don't leave jumper permanently as this would drain the battery.
(J11 JTAG)	Debug only, not populated.
(J12 PCI express)	Straddle mount PCI express (build option)
J13 USB	Internal USB (2 x USB 2.0)
J14 mSATA / miniPCI express	This slot can be used for mSATA SSD, or 3G/LTE modem (USB based). No PCI express = no wifi. Connects to SIM J2.
J15 miniPCI express	This slot can be used for 3G/LTE modems (USB based). No PCI express = no wifi. Connects to SIM J1.
J16 miniPCI express	This slot includes PCI express, and is intended for wifi modules. No SIM connected.
J17 USB	Internal USB (2 x USB 2.0)
(J18 LPC)	Test points for connection of LPC post code display.
(J19 NVM override)	Use to override NIC NVM write protect.
J20 GPIO	General purpose I/O pins + extra serial ports.
(J21 internal power)	Optional power header, designed for 0.156" pitch header (Digi-Key part A1971-ND).
J22 COM1	Serial port with full handshake signals.
J23 USB	External USB (2 x USB 3.0)
J24 Power	DC jack (2.5 mm center pin, center positive).
J25 LAN1	GigE port. Left LED (green) indicates activity, right LED (amber) is turned on when the connection is Gigabit.
J26 LAN2	GigE port
J27 LAN3	GigE port

Schematics

For detailed pinouts, full board schematics are available on our web site.

Hardware limitations

This board does not support power over Ethernet.

GPIO

The following signals are driven by the AMD FCH south bridge function:

Pushbutton switch S1 = G32

LED1 = G57, LED 2 = G58, LED 3 = G59

SIM switch is controlled by G33, 0 = swap, 1 = normal connection.

GPIO pins on header J20 are driven by the Nuvoton NCT5104D I/O controller. Data sheet and sample code available on request.

Operating system compatibility

Please keep in mind that apu boards do not include a keyboard controller. Some boot loaders may hang and need to be modified.

Please see our web site for up-to-date information.

FreeBSD

Recommend versions 10 and later.

FreeDOS

Tested ok, booting from SD card or USB stick.

CoreBoot is limited to two active USB storage devices, and does not react to kindly to hot plug events.

Linux

Please contact <u>support@pcengines.ch</u> for support if necessary. We provide sample images for tinyCore Linux at www.pcengines.ch/tinycore.htm. To access the thermal sensor under Voyage Linux:

apt-get install lm-sensors