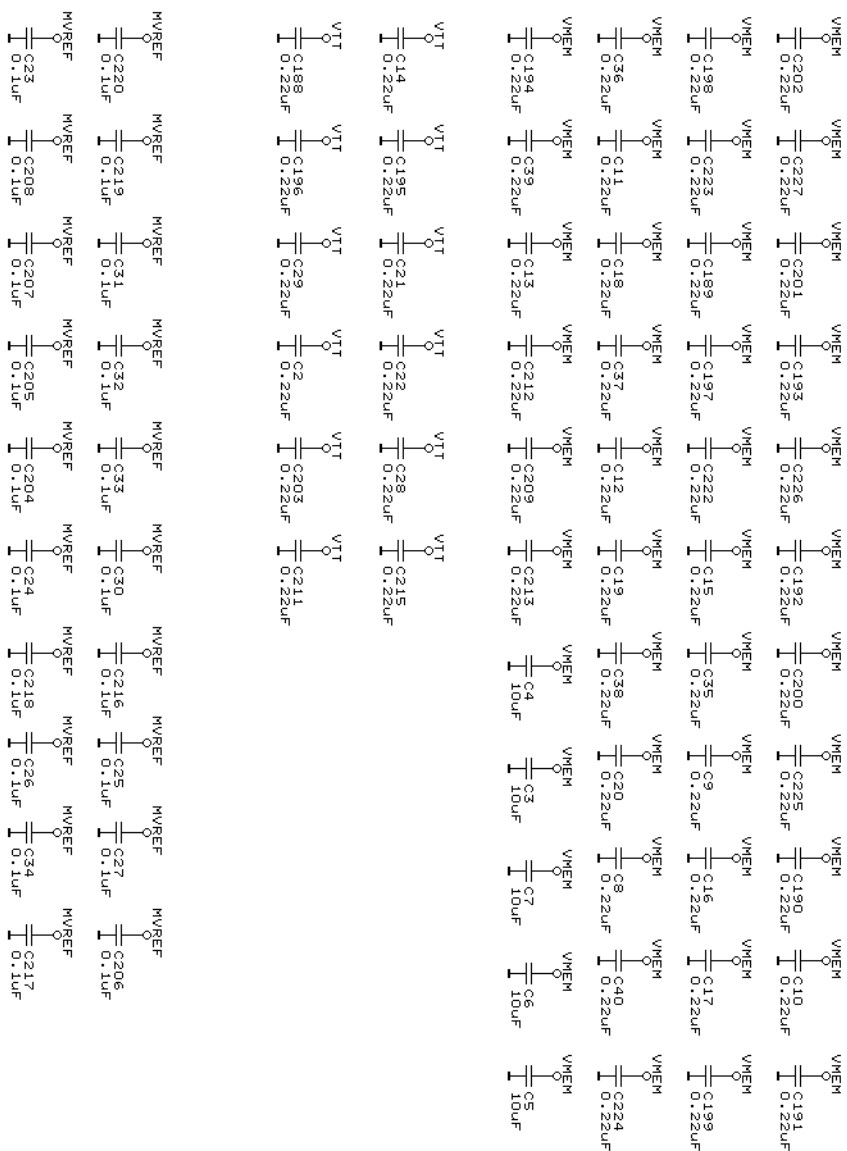


APU ground

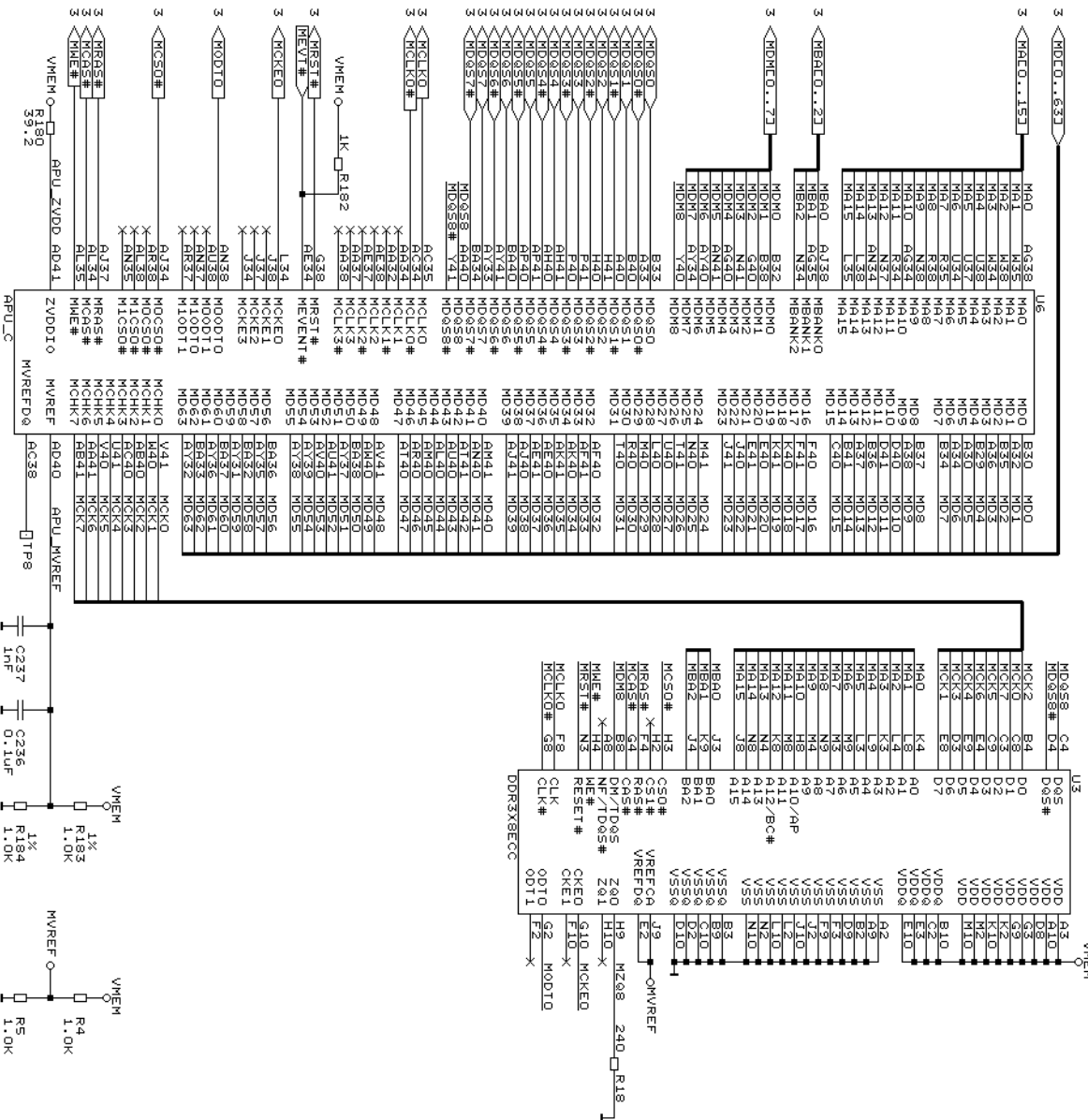
DRAM bypass

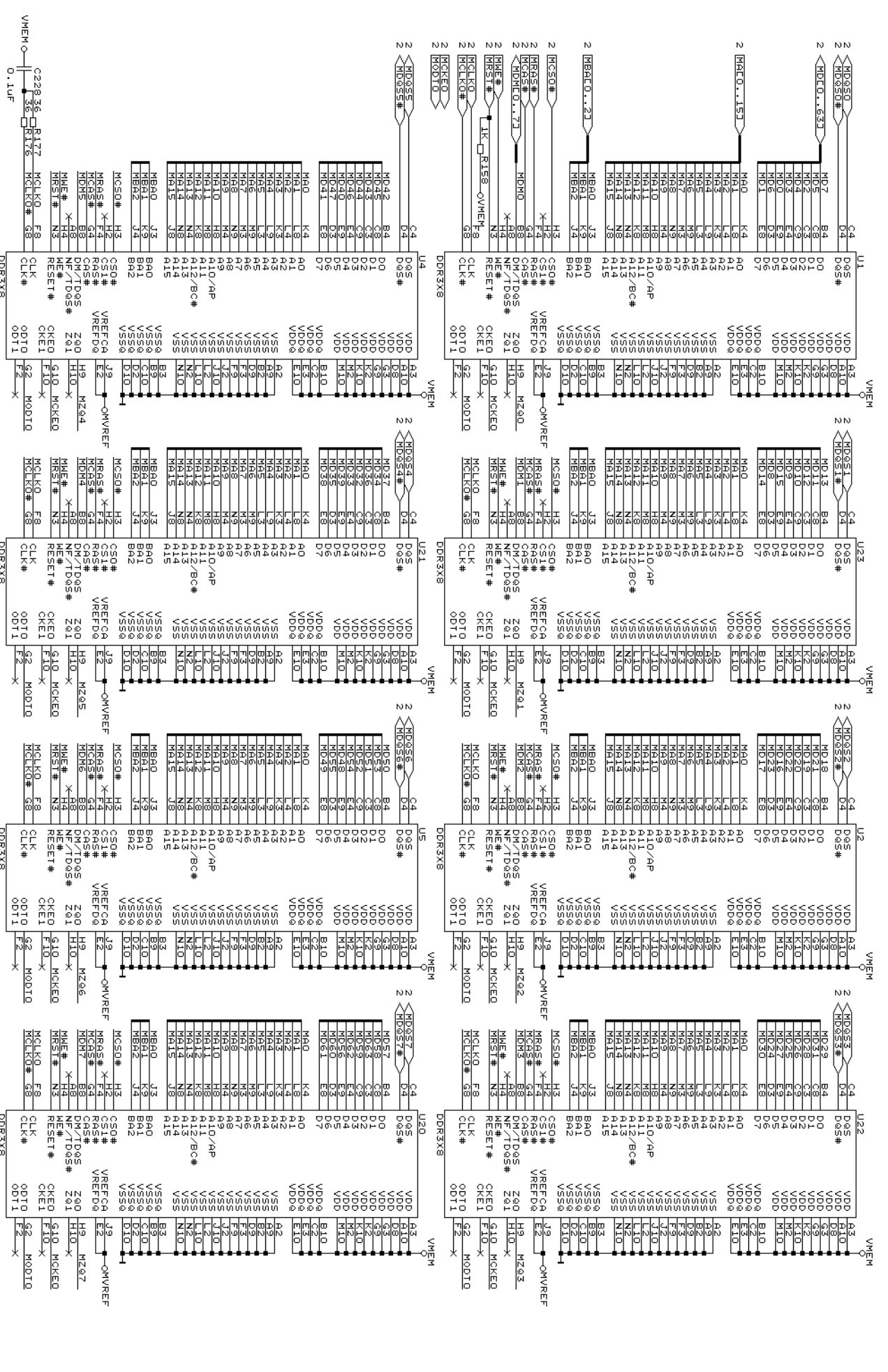


- 17.5SCH
- 15.5SCH
- 14.5SCH
- 12.5SCH
- 11.5SCH
- 10.5SCH
- 9.5SCH
- 8.5SCH
- 7.5SCH
- 6.5SCH
- 5.5SCH
- 4.5SCH
- 3.5SCH
- 2.5SCH
- 1.5SCH
- LNK

APU DRAM Interface

ECC DRAM





Memory Bank Addressing:

Bank U11: DRAM addresses 0x00000000-0x0000000F map to VMEH addresses 0x00000000-0x0000000F.

Bank U12: DRAM addresses 0x00000010-0x0000001F map to VMEH addresses 0x00000010-0x0000001F.

Bank U13: DRAM addresses 0x00000020-0x0000002F map to VMEH addresses 0x00000020-0x0000002F.

Bank U14: DRAM addresses 0x00000030-0x0000003F map to VMEH addresses 0x00000030-0x0000003F.

Bank U15: DRAM addresses 0x00000040-0x0000004F map to VMEH addresses 0x00000040-0x0000004F.

Bank U16: DRAM addresses 0x00000050-0x0000005F map to VMEH addresses 0x00000050-0x0000005F.

Bank U17: DRAM addresses 0x00000060-0x0000006F map to VMEH addresses 0x00000060-0x0000006F.

Bank U18: DRAM addresses 0x00000070-0x0000007F map to VMEH addresses 0x00000070-0x0000007F.

Bank U19: DRAM addresses 0x00000080-0x0000008F map to VMEH addresses 0x00000080-0x0000008F.

Bank U20: DRAM addresses 0x00000090-0x0000009F map to VMEH addresses 0x00000090-0x0000009F.

Chip Selects: CS0, CS1, CS2, CS3 are used to select the bank. CS0 is active-low. CS1, CS2, CS3 are active-low.

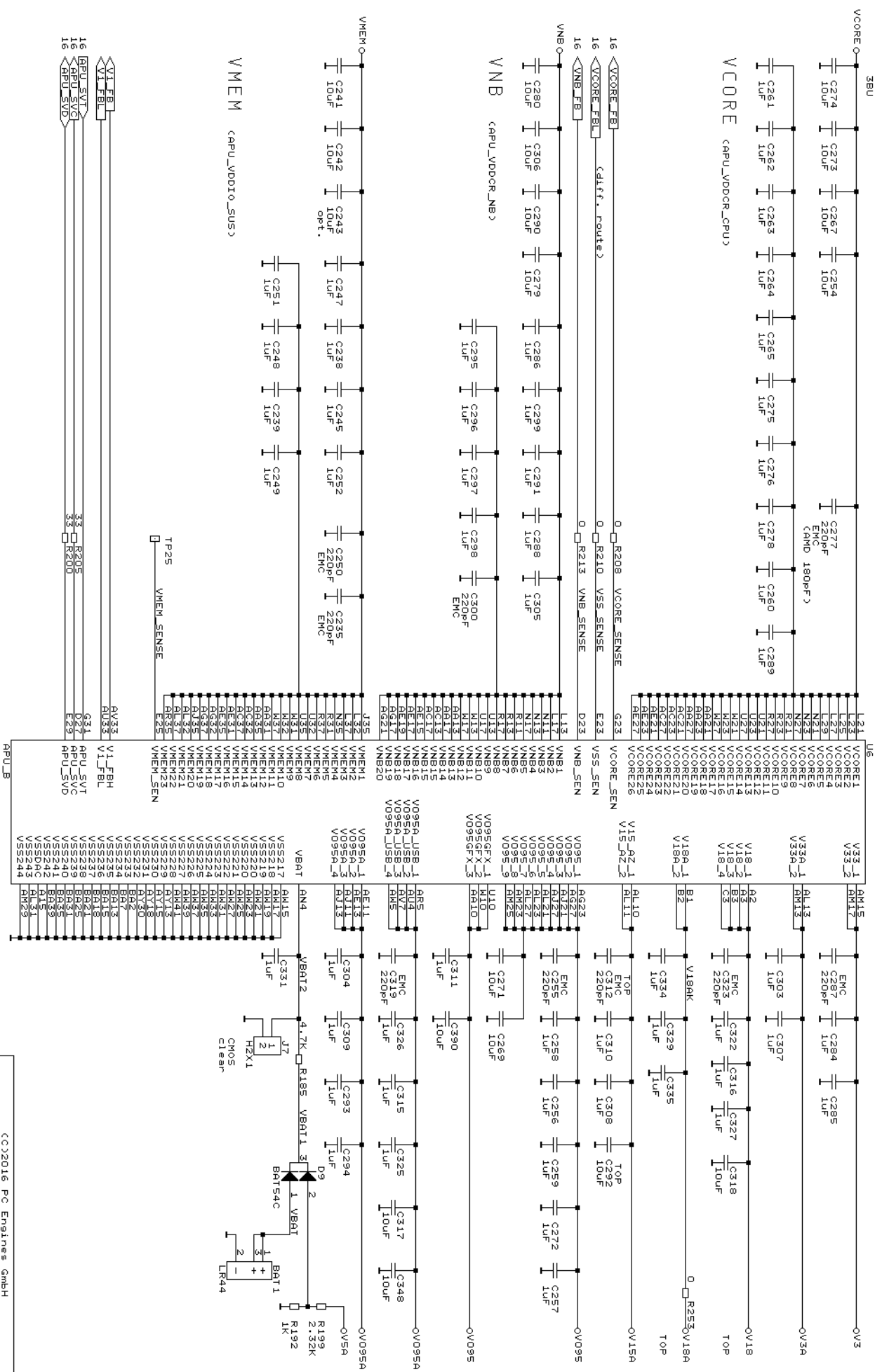
Row Address: R0-R15 are used to address the rows within each channel. R0-R15 are active-low.

Column Address: C0-C3 are used to address the columns within each channel. C0-C3 are active-low.

Control Signals: OE1, CE1, F2 are used for control. OE1 is active-low. CE1 is active-low. F2 is active-low.

Memory Bank Addressing: Bank U11: DRAM addresses 0x00000000-0x0000000F map to VMEH addresses 0x00000000-0x0000000F. Bank U12: DRAM addresses 0x00000010-0x0000001F map to VMEH addresses 0x00000010-0x0000001F. Bank U13: DRAM addresses 0x00000020-0x0000002F map to VMEH addresses 0x00000020-0x0000002F. Bank U14: DRAM addresses 0x00000030-0x0000003F map to VMEH addresses 0x00000030-0x0000003F. Bank U15: DRAM addresses 0x00000040-0x0000004F map to VMEH addresses 0x00000040-0x0000004F. Bank U16: DRAM addresses 0x00000050-0x0000005F map to VMEH addresses 0x00000050-0x0000005F. Bank U17: DRAM addresses 0x00000060-0x0000006F map to VMEH addresses 0x00000060-0x0000006F. Bank U18: DRAM addresses 0x00000070-0x0000007F map to VMEH addresses 0x00000070-0x0000007F. Bank U19: DRAM addresses 0x00000080-0x0000008F map to VMEH addresses 0x00000080-0x0000008F. Bank U20: DRAM addresses 0x00000090-0x0000009F map to VMEH addresses 0x00000090-0x0000009F.

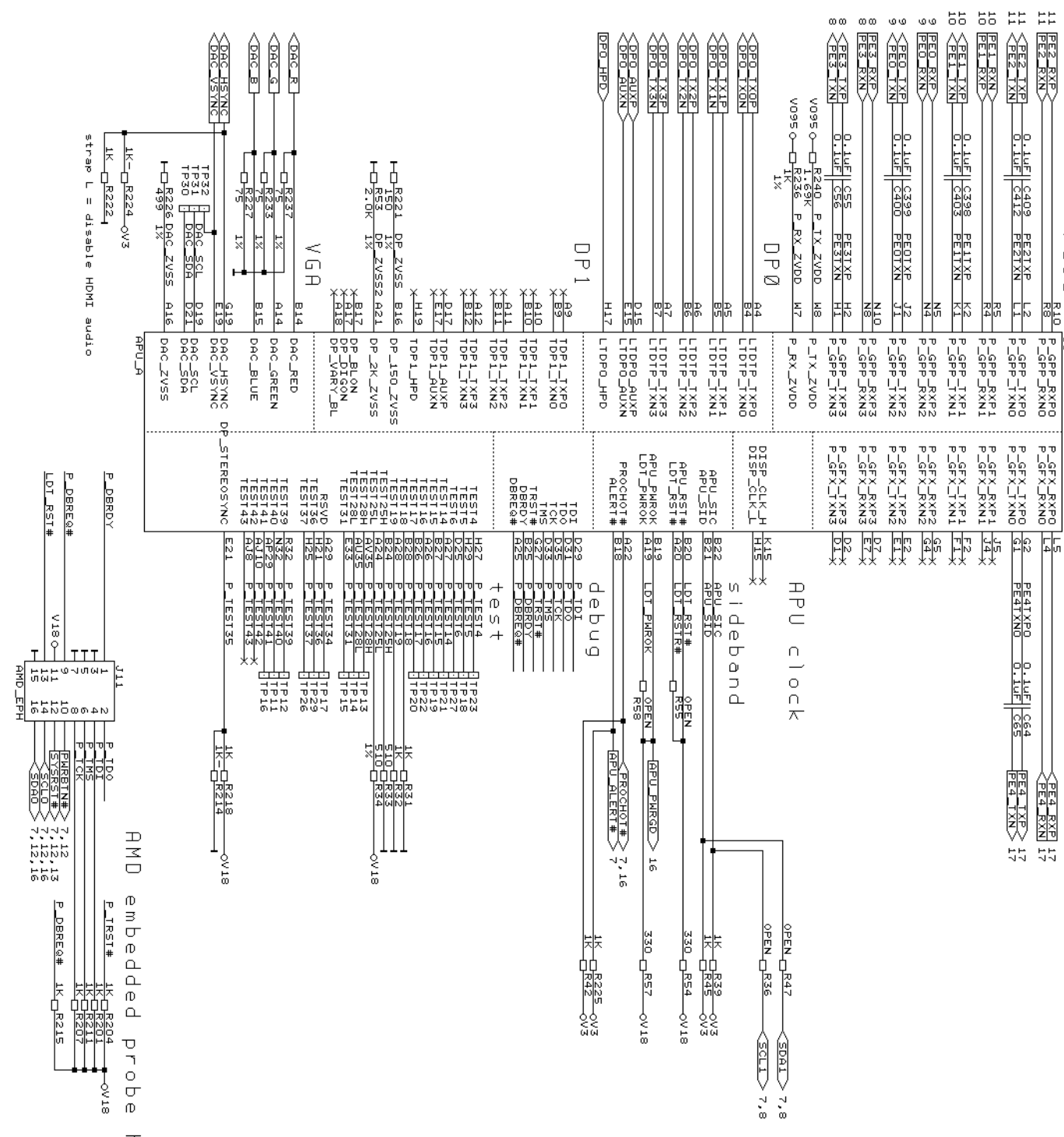
APU power



PCIe

APU

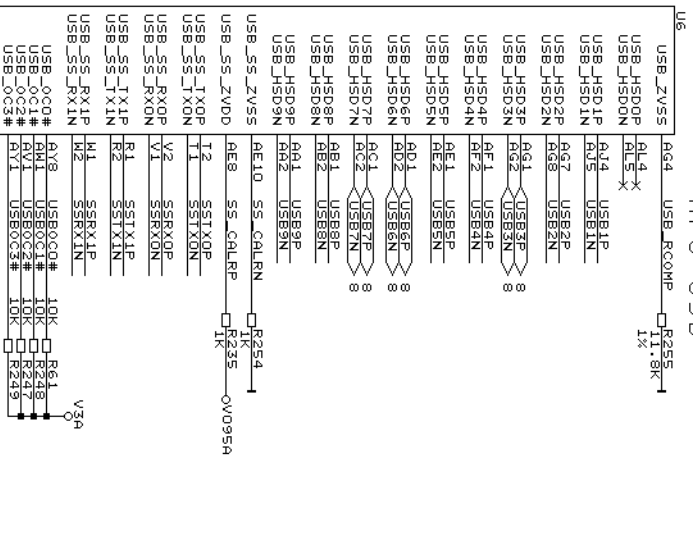
PCIe x 4



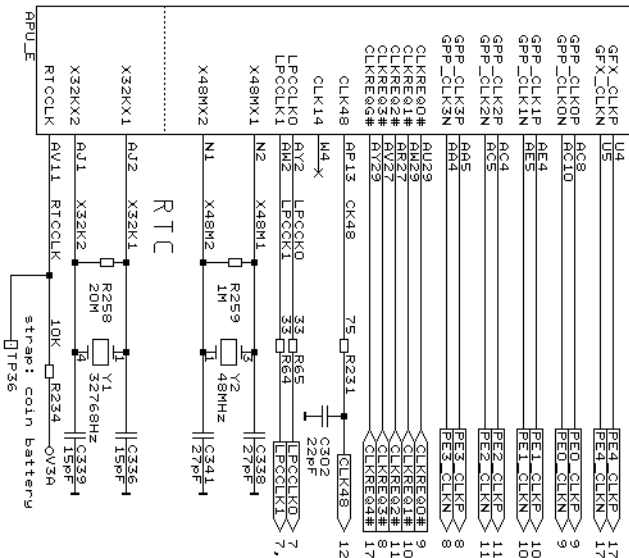
AMD embedded probe header

Title	APU PCIe / display / test
Size	Document Number
Rev	APU
Date:	May 29, 2018 Sheet 5 of 17

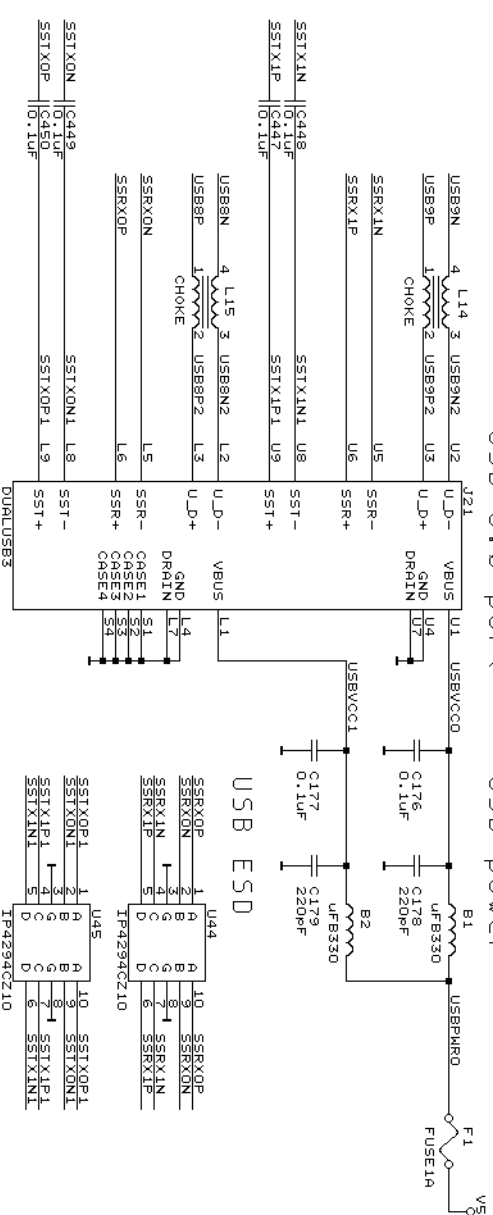
APU USB



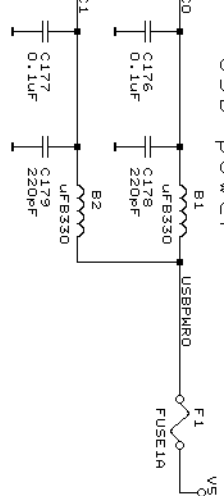
APU clock



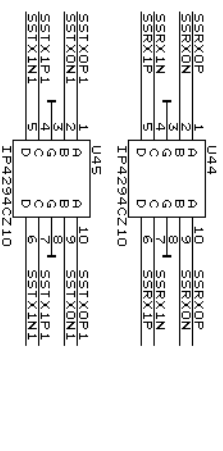
USB 3.0 port



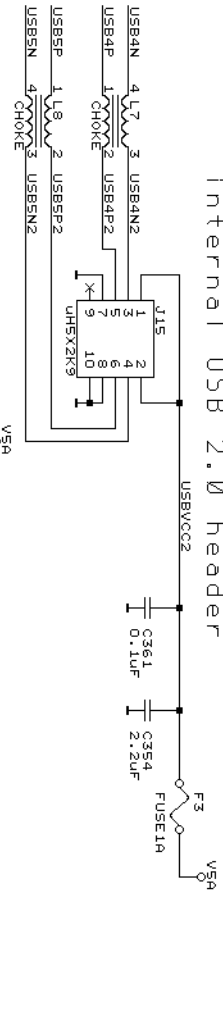
USB power



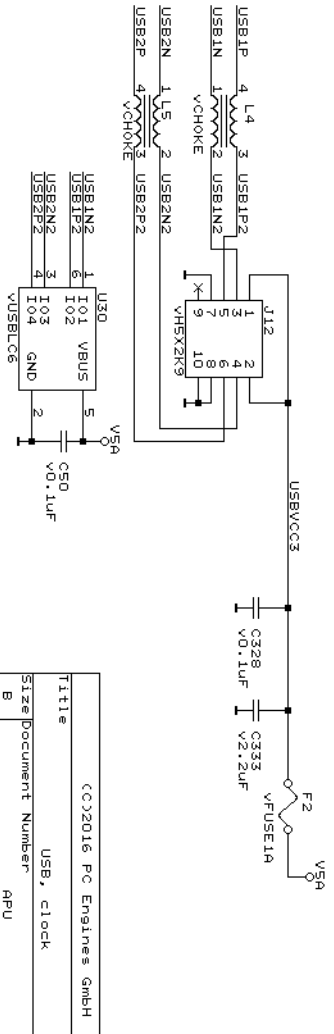
USB ESD

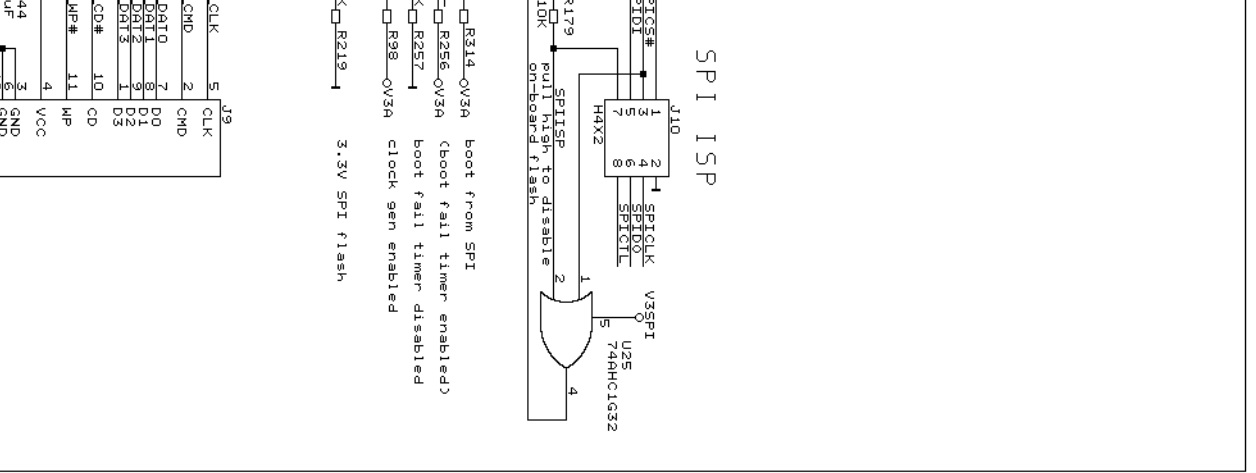
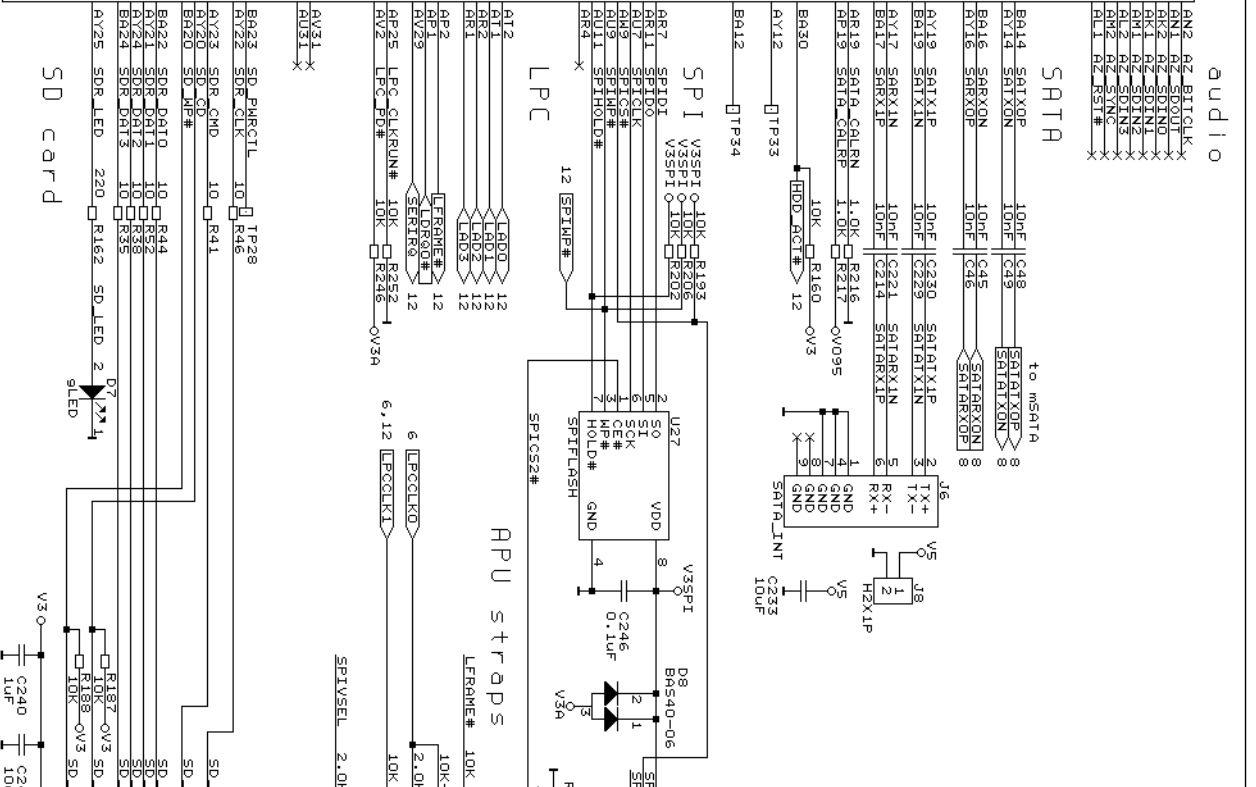
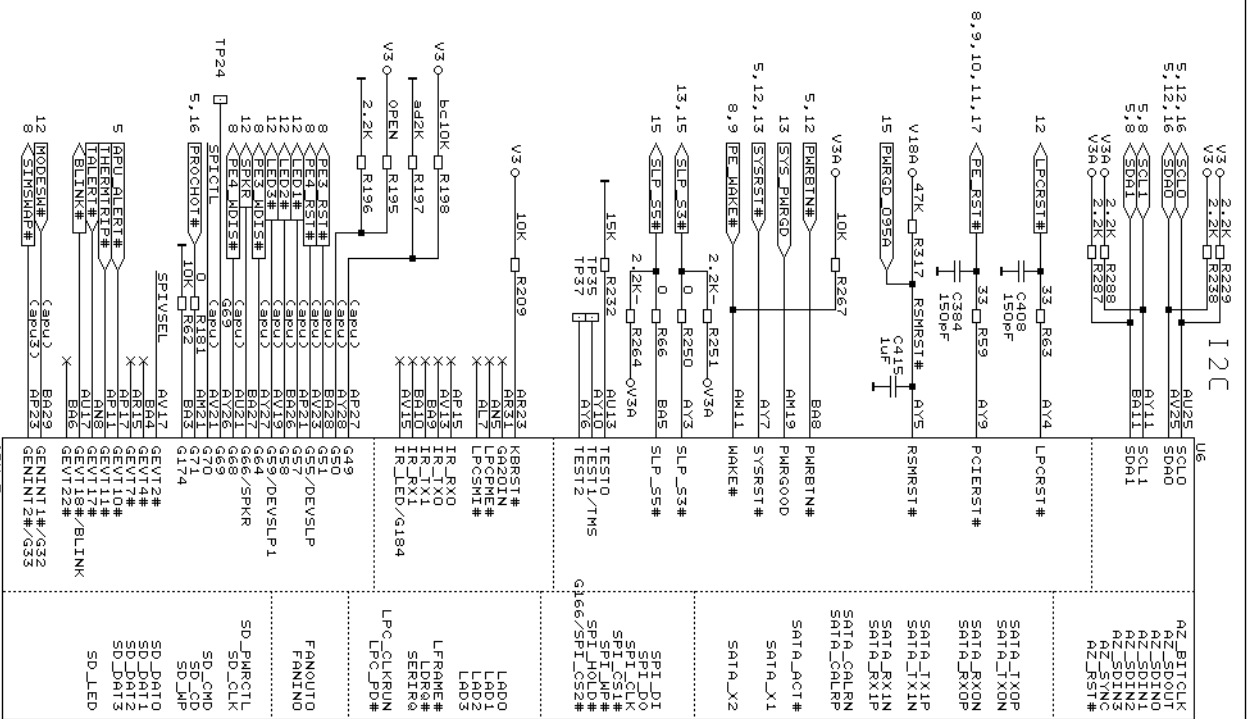


Internal USB 2.0 header

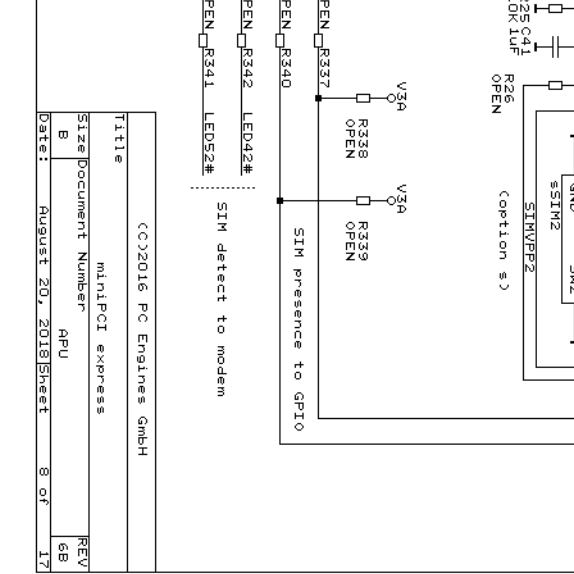
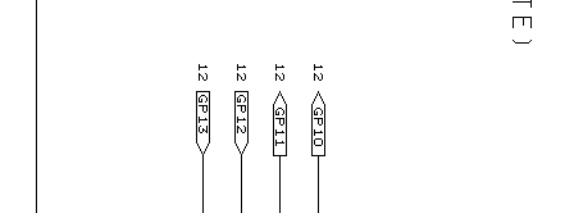
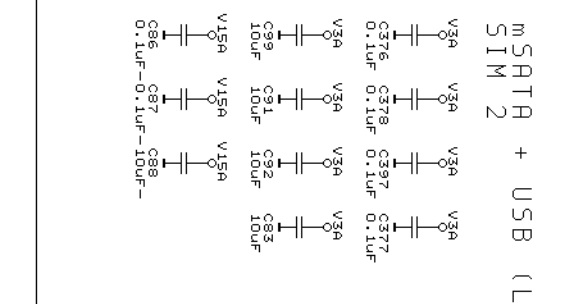
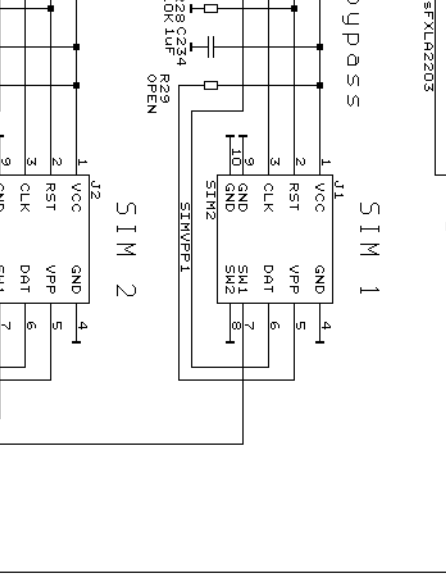
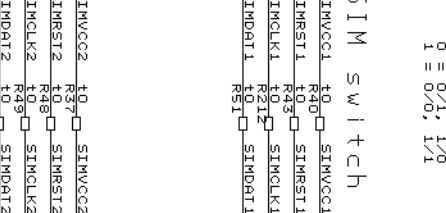
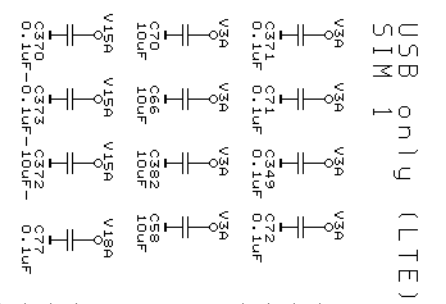
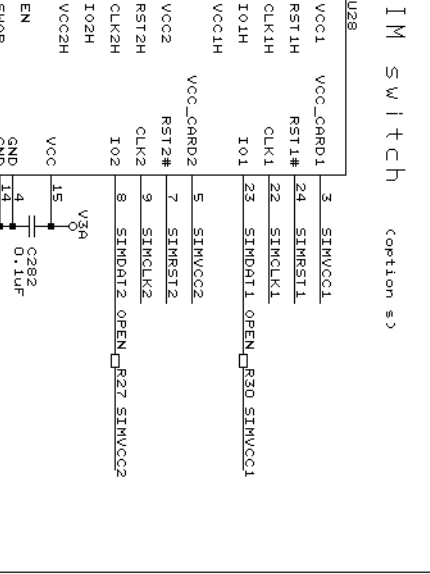
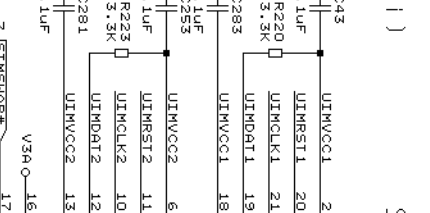
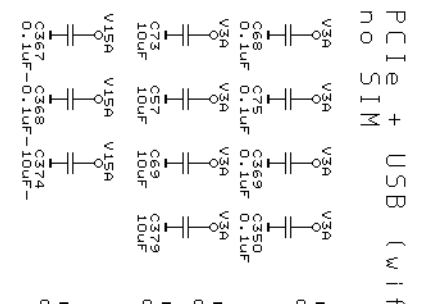
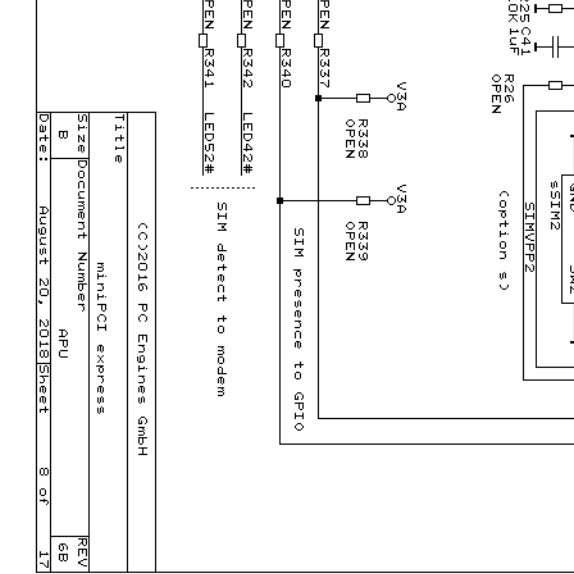
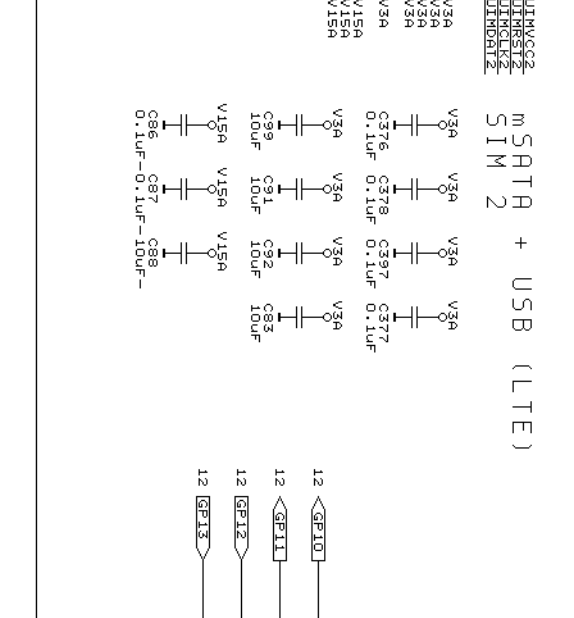
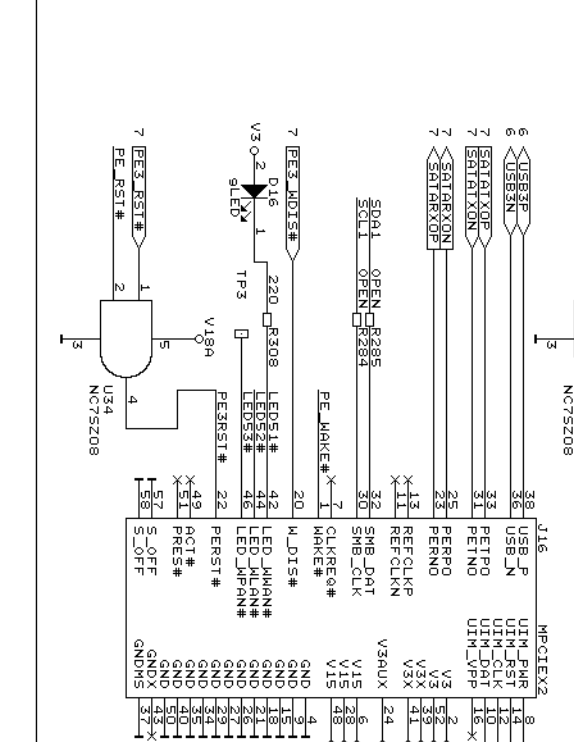
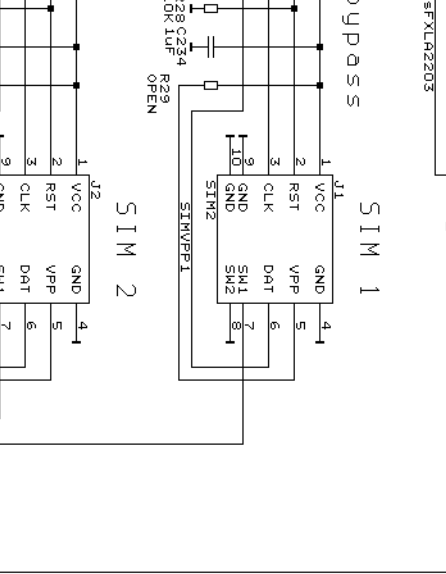
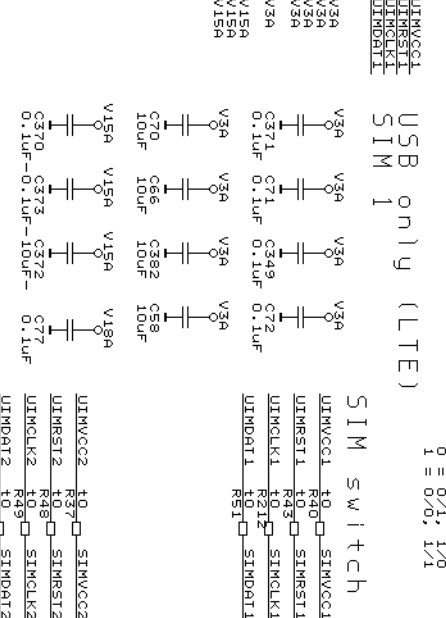
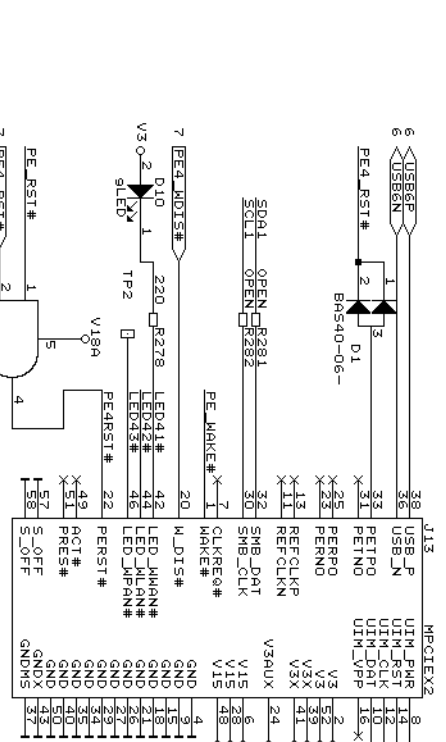
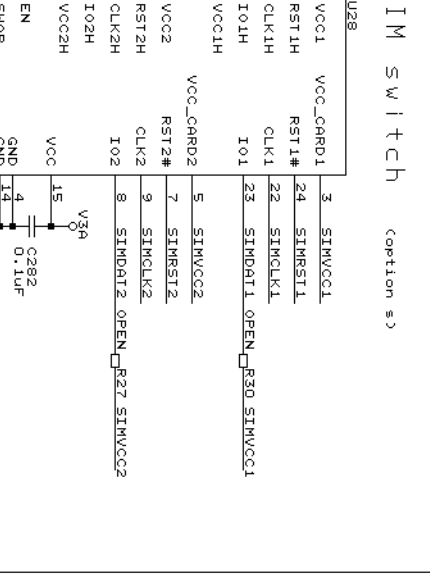
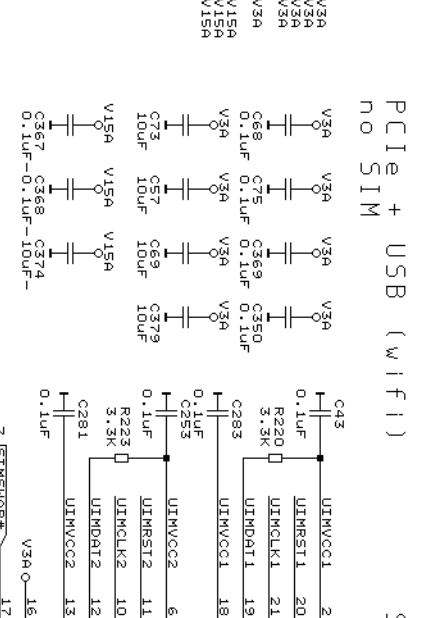
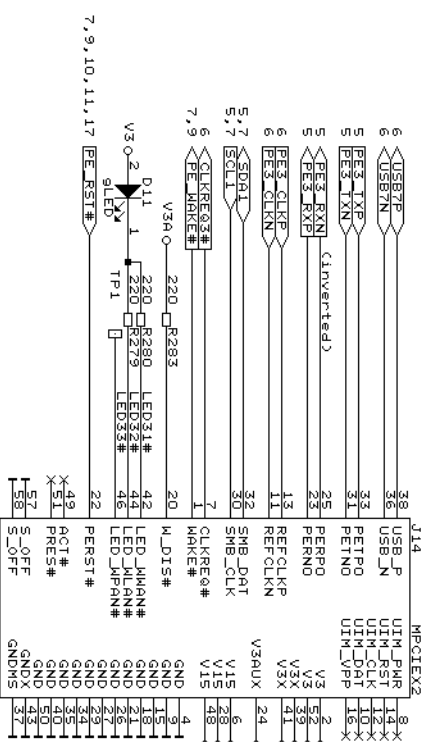


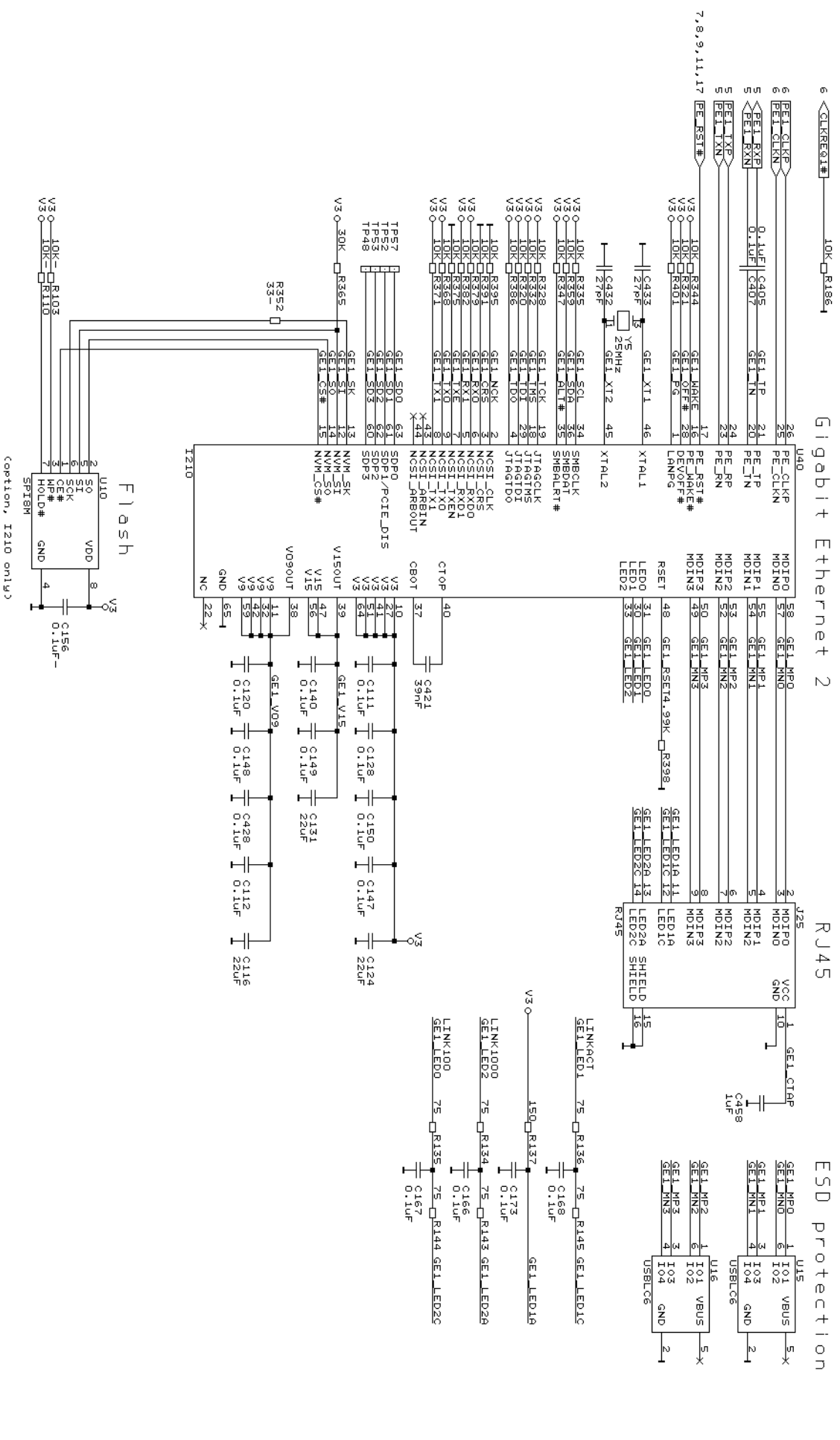
Internal USB 2.0 header (option v)





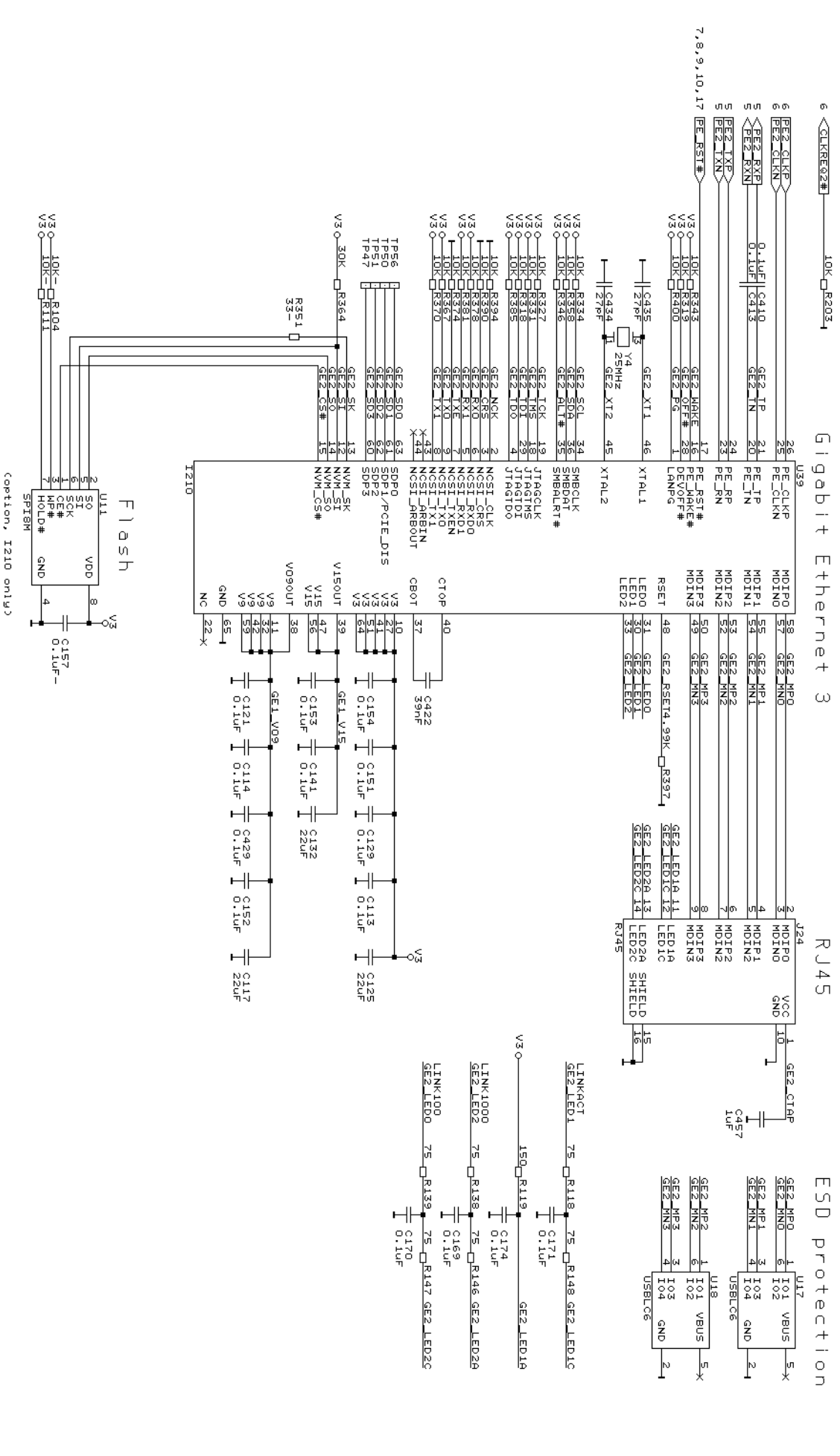
GPIO	APU	SD card
AV17	GEVT2#	SD_D0
AV18	GEVT2#	SD_D1
AV19	GEVT4#	SD_D2
AV20	GEVT4#	SD_D3
AV21	GEVT10#	SD_D4
AV22	GEVT10#	SD_D5
AV23	GEVT17#	SD_D6
AV24	GEVT18#	SD_D7
AV25	GEVT18#	SD_D8
AV26	GEVT22#	SD_D9
AV27	GEVT22#	SD_D10
AV28	GENINT1#/CS3	SD_D11
AV29	GENINT2#/CS3	SD_D12
AV30		SD_D13
AV31		SD_D14
AV32		SD_D15
AV33		SD_D16
AV34		SD_D17
AV35		SD_D18
AV36		SD_D19
AV37		SD_D20
AV38		SD_D21
AV39		SD_D22
AV40		SD_D23
AV41		SD_D24
AV42		SD_D25
AV43		SD_D26
AV44		SD_D27
AV45		SD_D28
AV46		SD_D29
AV47		SD_D30
AV48		SD_D31
AV49		SD_D32
AV50		SD_D33
AV51		SD_D34
AV52		SD_D35
AV53		SD_D36
AV54		SD_D37
AV55		SD_D38
AV56		SD_D39
AV57		SD_D40
AV58		SD_D41
AV59		SD_D42
AV60		SD_D43
AV61		SD_D44
AV62		SD_D45
AV63		SD_D46
AV64		SD_D47
AV65		SD_D48
AV66		SD_D49
AV67		SD_D50
AV68		SD_D51
AV69		SD_D52
AV70		SD_D53
AV71		SD_D54
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AV73		SD_D56
AV74		SD_D57
AV75		SD_D58
AV76		SD_D59
AV77		SD_D60
AV78		SD_D61
AV79		SD_D62
AV80		SD_D63
AV81		SD_D64
AV82		SD_D65
AV83		SD_D66
AV84		SD_D67
AV85		SD_D68
AV86		SD_D69
AV87		SD_D70
AV88		SD_D71
AV89		SD_D72
AV90		SD_D73
AV91		SD_D74
AV92		SD_D75
AV93		SD_D76
AV94		SD_D77
AV95		SD_D78
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AV97		SD_D80
AV98		SD_D81
AV99		SD_D82
AV100		SD_D83





(option, I210 only)

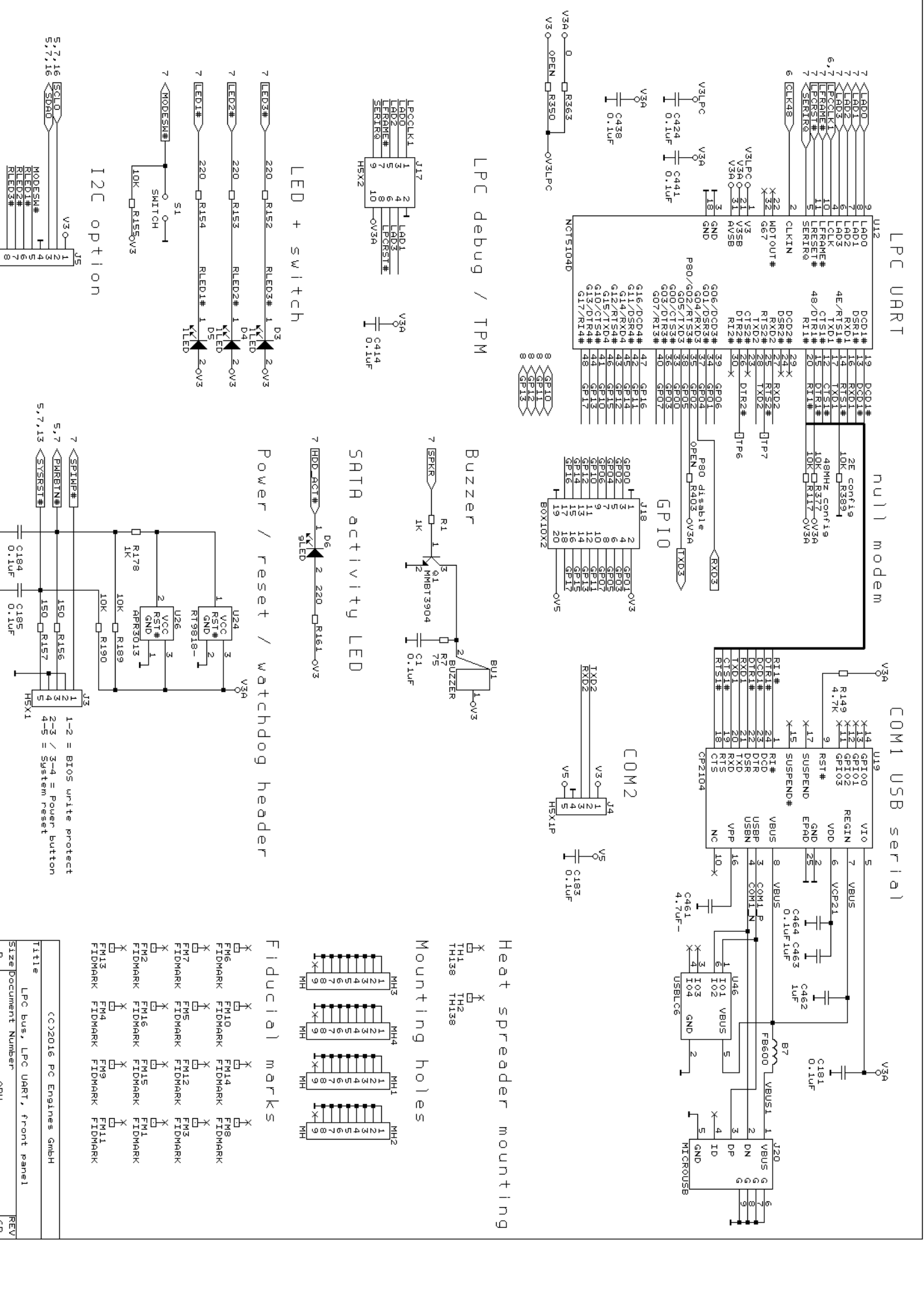
Title		Ethernet (2)	
Size/Document Number		APU	
Date:		May 30, 2018/Sheet 10 of 17	
REV		68	
©2016 PC Engines GmbH			



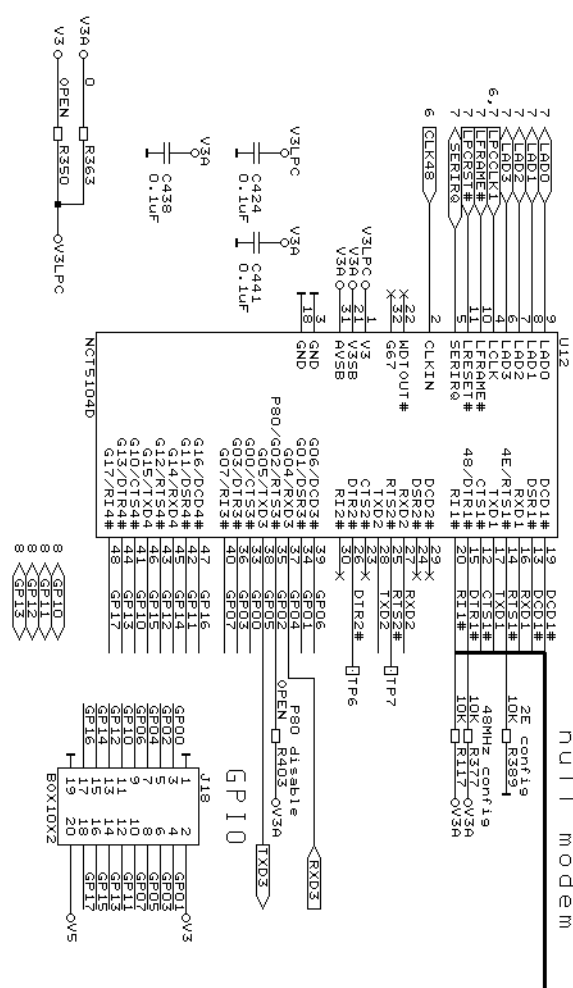
Flash

(option, I210 only)

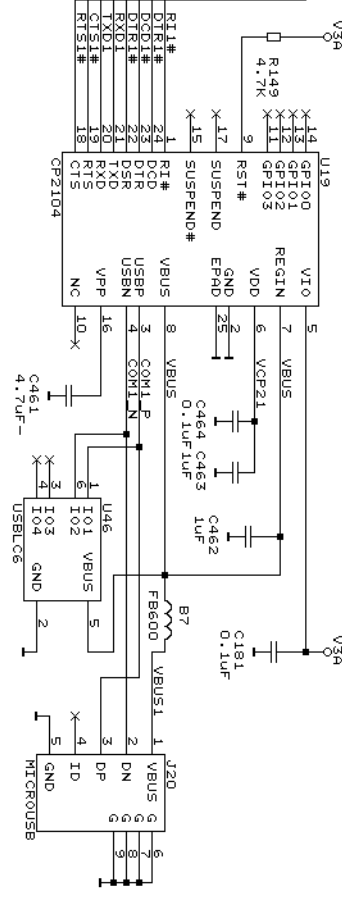
©2016 PC Engines GmbH	
Title	Ethernet (3)
Size Document Number	APU
B	REV
Date: May 30, 2018	Sheet 11 of 17



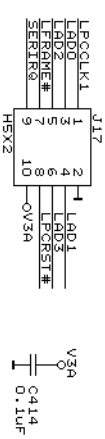
LPC UART



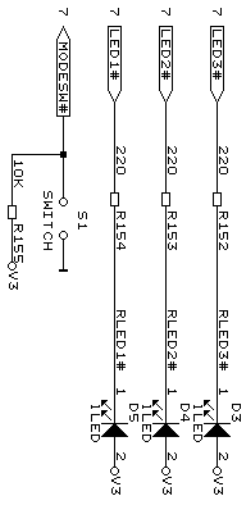
COM1 USB serial



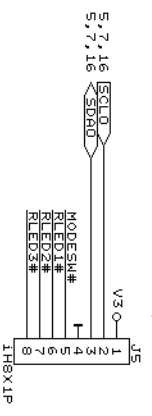
LPC debug / TPM



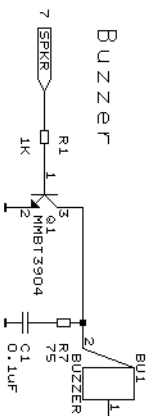
LED + switch



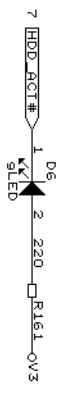
I2C option



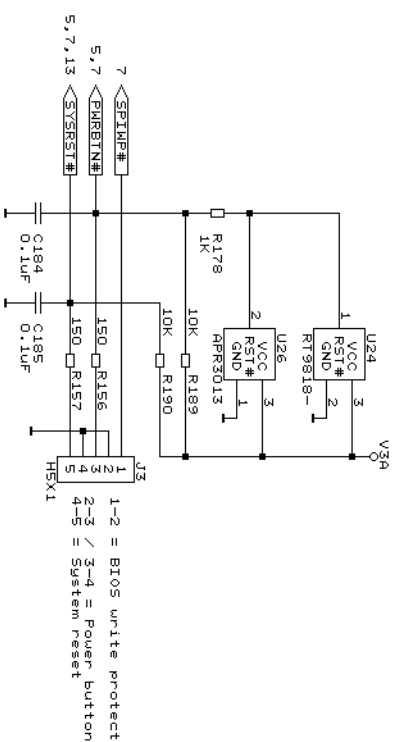
Buzzer



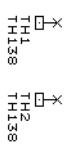
SATR activity LED



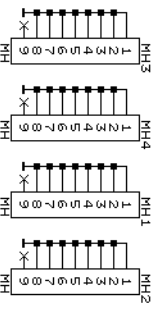
Power / reset / watchdog header



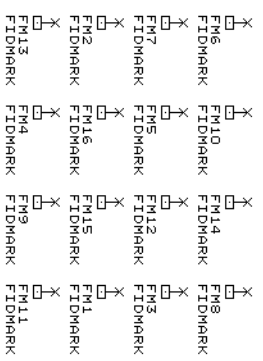
Heat spreader mounting



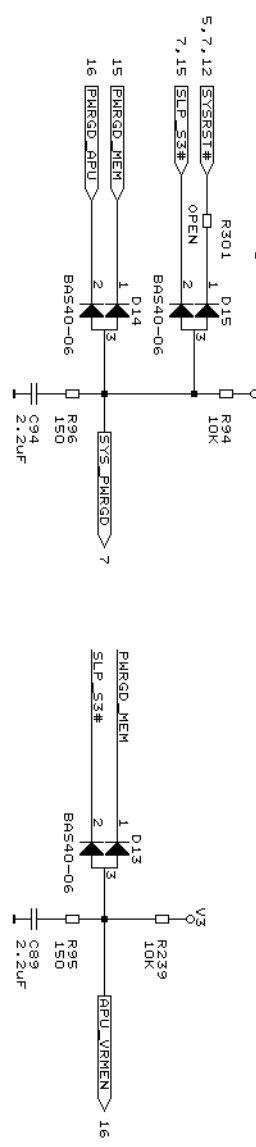
Mounting holes



Fiducial marks



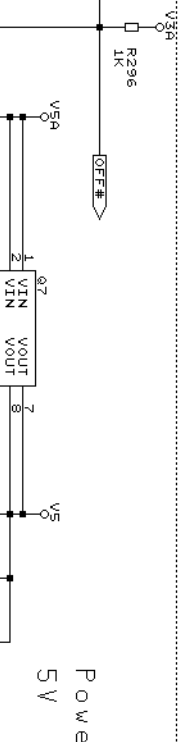
Power good visa



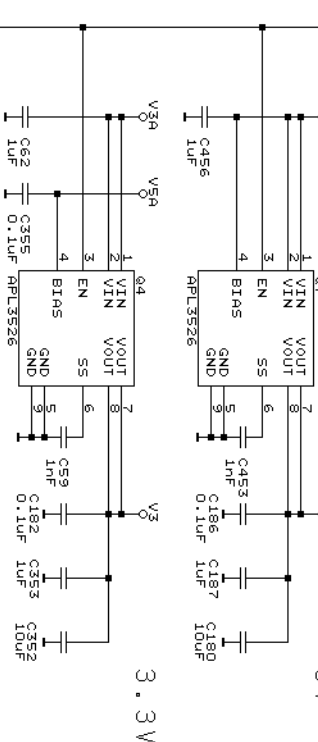
VRM test points

- V5A-O-TP59
- V5-O-TP60
- V3A-O-TP46
- V3-O-TP45
- V18A-O-TP39
- V18-O-TP38
- V15A-O-TP42
- V11-O-TP9
- V095A-O-TP44
- V095-O-TP43
- VCORE-O-TP40
- VNB-O-TP41

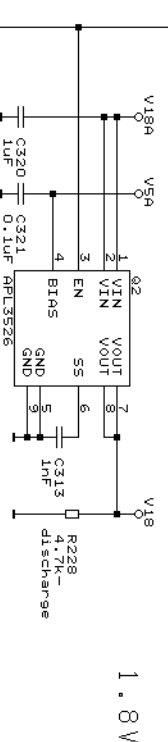
PARGD_MEM 1
SLP_S3# 2
BAS40-06
OFF#
D12



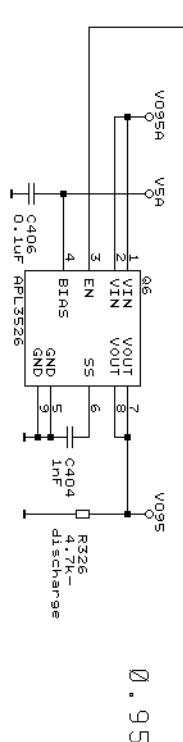
Power switch
5V



3.3V



1.8V

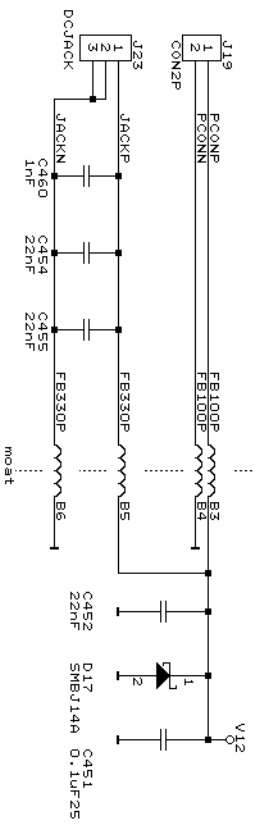


0.95V

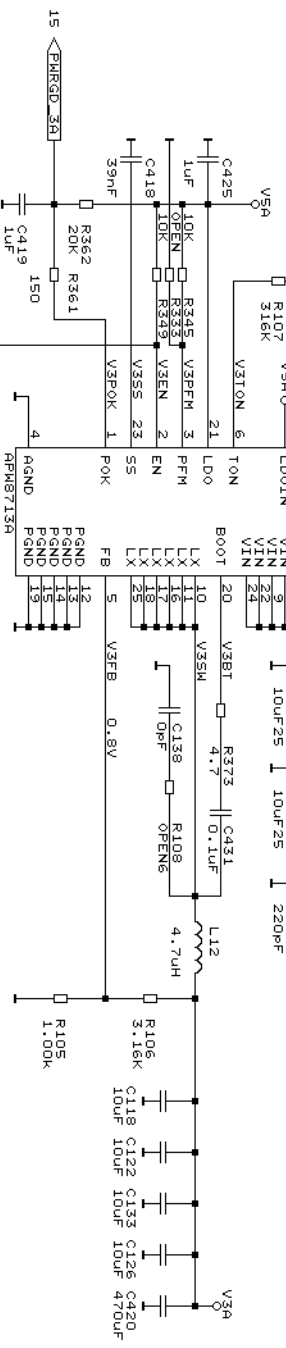
Title		power good, power switch	
Size/Document Number		APU	
REV		68	
Date:		August 28, 2018	
Sheet		13 of 17	

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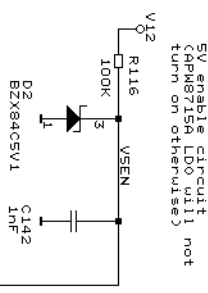
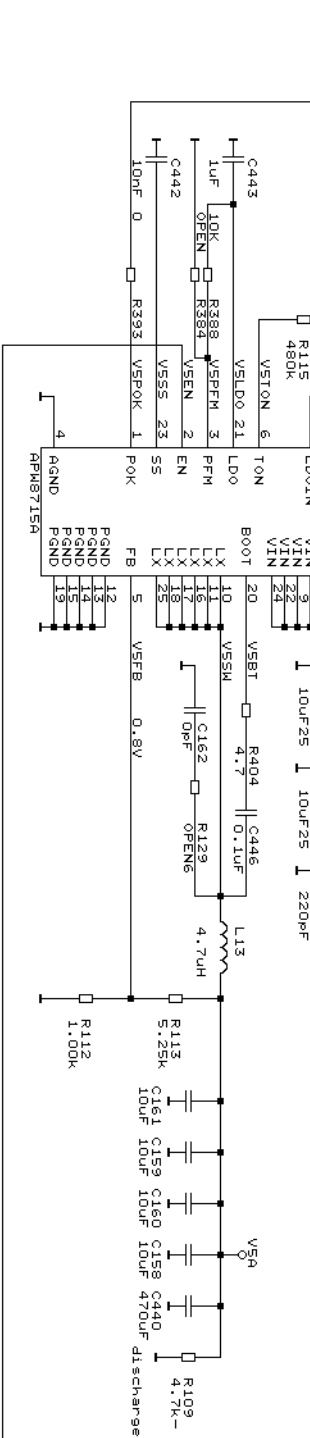
Power input +12V



3.3V regulator

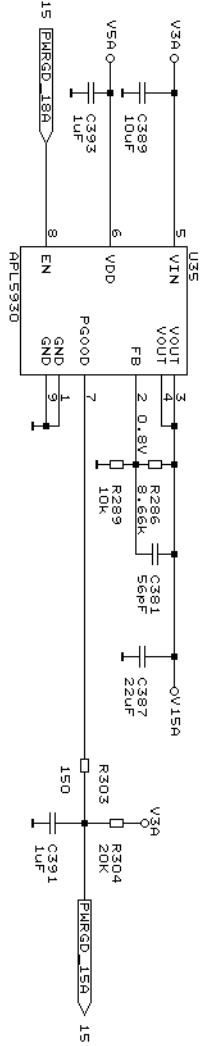


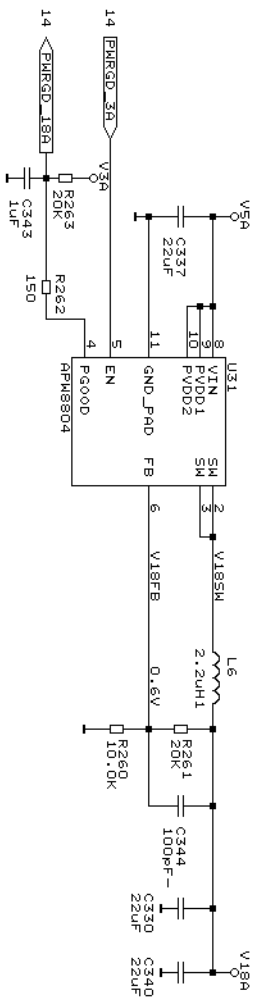
5V regulator



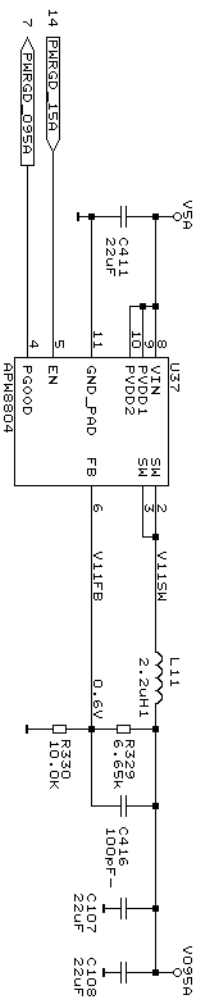
5V enable circuit (APM8715A LDO will turn on otherwise)

3.3V -> 1.5V LDO (0.5A)



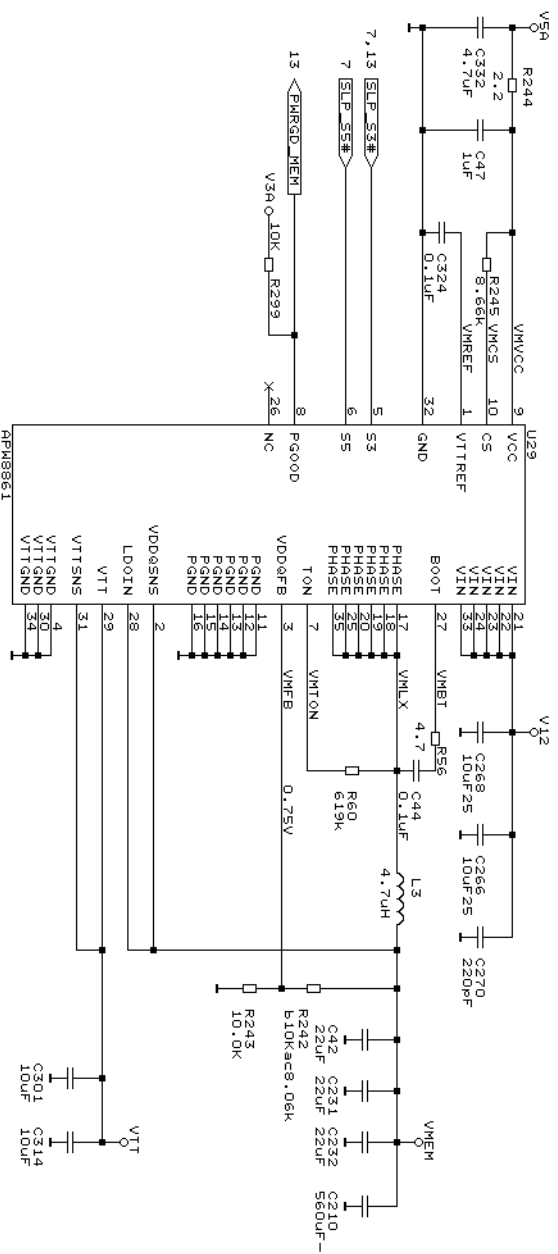


1.8 V , 2A



0.95A , 3A

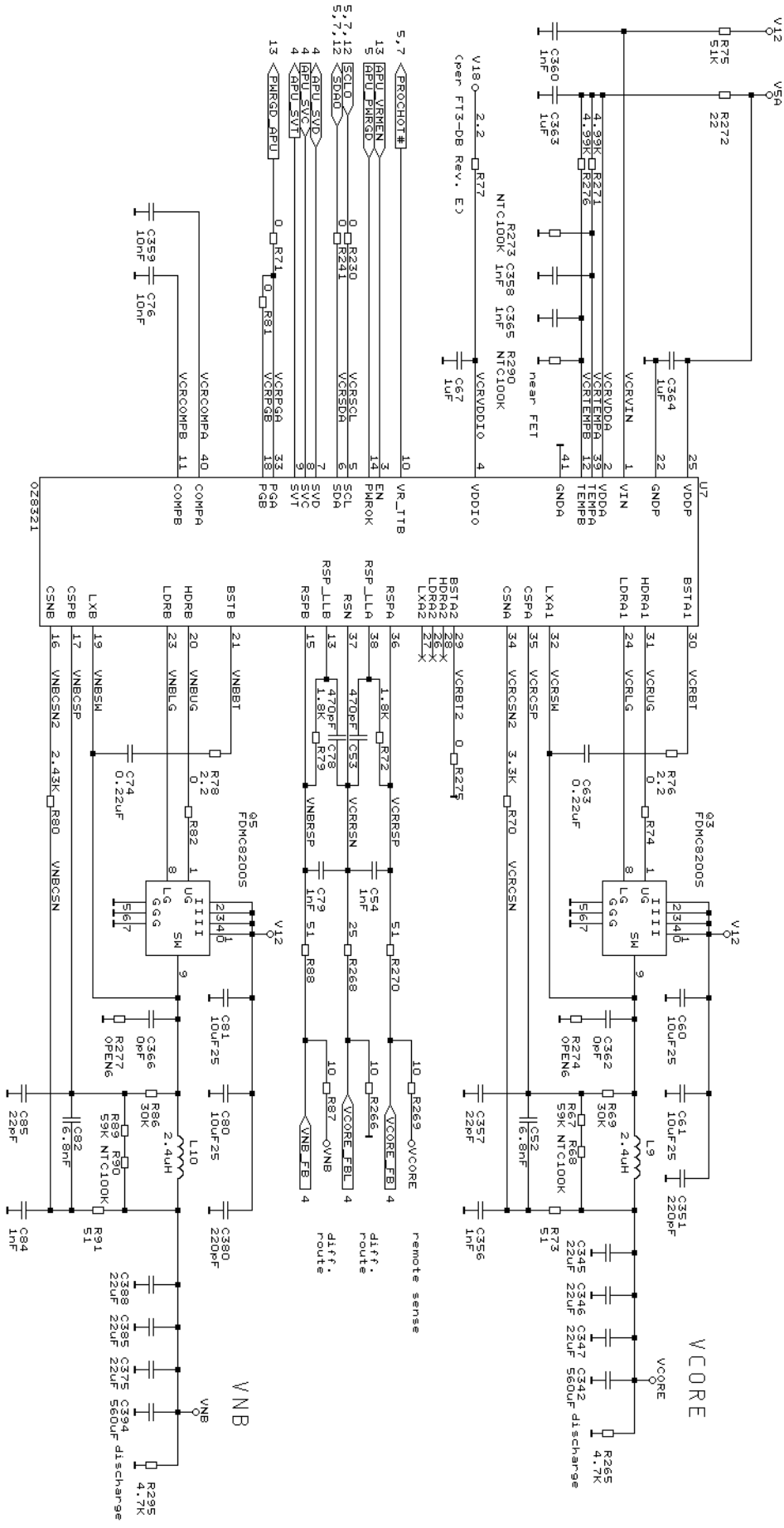
VMEM converter and VTT LDO



1.5V / 1.35V VMEM
0.75V / 0.675V VTT

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Title	1.8V, 0.95V, VMEM, VTT
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VCORE and VNB converter



Title		VCORE, VNB	
Size/Document Number		APU	
Date:		May 25, 2020	
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Gigabit Ethernet 4

